

# BMW Z4 14" Schematics Document

## Ivy/Sandy Bridge Panther Point

**2012-04-02**

**REV : A00**

*DY : None Installed*

*UMA: UMA only installed*

*SG: PX solution installed.*

<Core Design>



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Title

**Cover Page**

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Document Number

**BMW Z4 DIS**

Rev

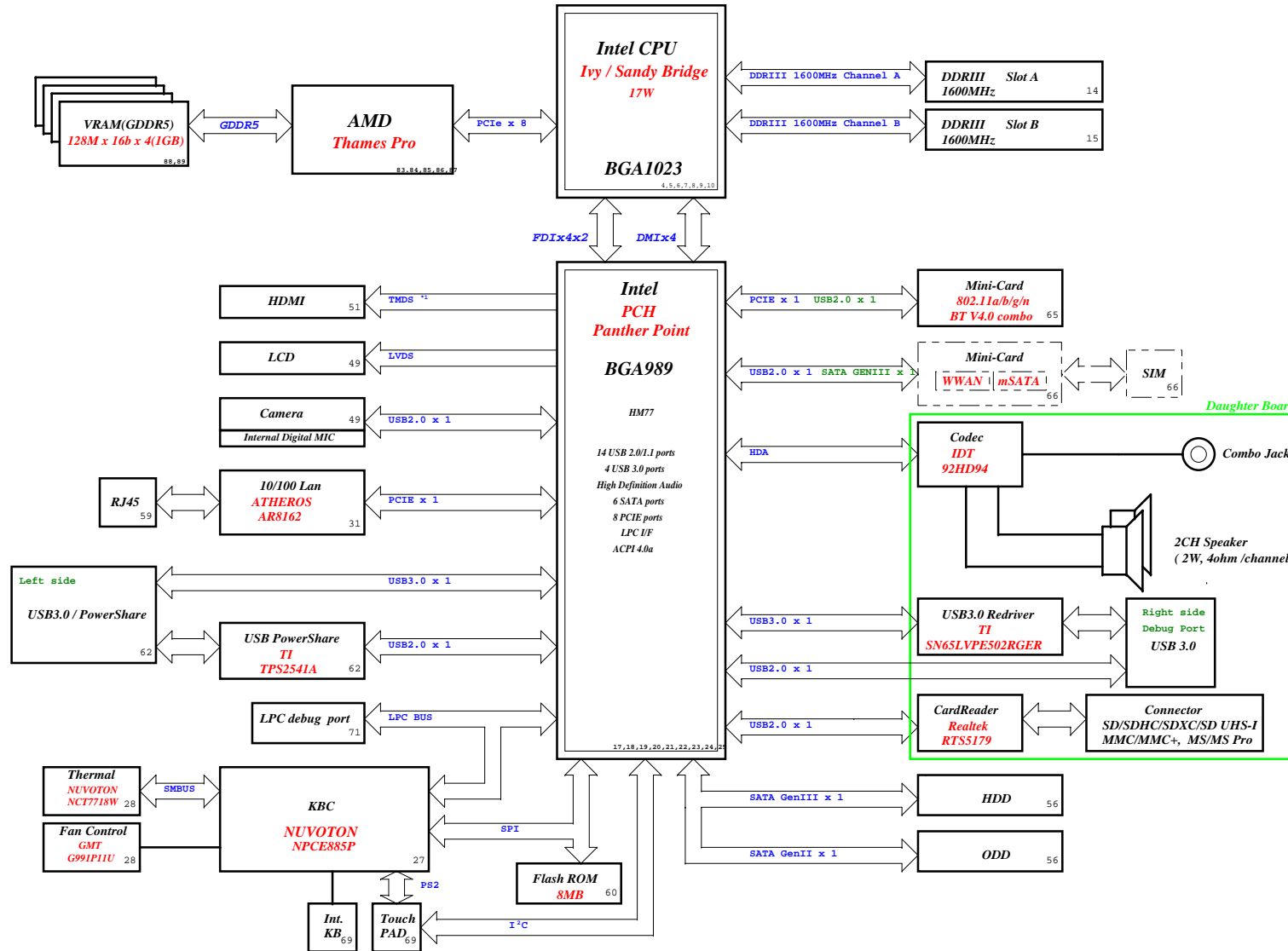
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Date: Monday, April 02, 2012

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# Block Diagram (Discrete / UMA)

Project Code: 91.4UV01.001  
PCB P/N : 48.4SB02.011  
Revision : 11289-1



| CHARGER  |  | 40    |
|--|--|-------|
| BQ24727  |  |       |
| INPUTS   | OUTPUTS  |       |
| AD+  | BT+  |       |
| SYSTEM DC/DC   |  | 41    |
| TPS51125RGER   |  |       |
| INPUTS   | OUTPUTS  |       |
| DCBATOUT   | 5V_AUX_S5<br>3D3V_AUX_S5<br>5V_S5<br>3D3V_S5<br>15V_S5                                     |       |
| CPU DC/DC  |  | 42,43 |
| VT1318+VT1326  |  |       |
| INPUTS   | OUTPUTS  |       |
| 5V_S5  | VCC_CORE   |       |
| GFX DC/DC  |  | 44    |
| VT1318+VT1323  |  |       |
| INPUTS   | OUTPUTS  |       |
| 5V_S5  | VCC_GFXCORE  |       |
| SYSTEM DC/DC   |  | 45    |
| VT386  |  |       |
| INPUTS   | OUTPUTS  |       |
| 5V_S5  | 1D05V_PCH<br>VCCP_CPU  |       |
| SYSTEM DC/DC   |  | 46    |
| VT385(DIS)/RT9026<br>VT386(UMA)/RT9026                       |  |       |
| INPUTS   | OUTPUTS  |       |
| DCBATOUT   | 1D5V_S3<br>0D75V_S0<br>DDR_VREF_S3   |       |
| SYSTEM DC/DC   |  | 47    |
| RT8068A  |  |       |
| INPUTS   | OUTPUTS  |       |
| 3D3V_S5  | 1D8V_S0  |       |
| SYSTEM DC/DC   |  | 48    |
| APL5916  |  |       |
| INPUTS   | OUTPUTS  |       |
| VCCP_CPU   | 0D85_S0  |       |
| VGA DC/DC  |  | 92    |
| VT358  |  |       |
| INPUTS   | OUTPUTS  |       |
| 5V_S5  | VGA_CORE   |       |
| VGA DC/DC  |  | 93    |
| APL5930  |  |       |
| INPUTS   | OUTPUTS  |       |
| 1D5V_S3  | 1V_VGA_S0  |       |
| Switches   |  |       |
| INPUTS   | OUTPUTS  |       |
| 1D5V_S3<br>5V_S5<br>3D3V_S5<br>3D3V_S5<br>1D8V_S0<br>1D5V_S3 | 1D5V_S0<br>5V_S0<br>3D3V_S0<br>3D3V_MLAN_ACAC<br>3D3V_VGA_S0<br>1D8V_VGA_S0<br>1D5V_VGA_S0 |       |
| UMA/Discrete   |  |       |
| PCB LAYER  |  |       |
| L1:Top<br>L2:GND<br>L3:Signal<br>L4:Signal                   | L5:VCC<br>L6:Signal<br>L7:GND<br>L8:Bottom   |       |

\*1: Transition minimized differential signaling

PCH Strapping

| Name   | Schematics Notes   |
|--|--|
| SPKR   | The signal has a weak internal pull-down.<br>If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).   |
| INIT3_3V#                                    | Weak internal pull-up. Leave as "No Connect".  |
| INTVRMEN                                     | Integrated 1 V VRMs is enabled when high, External when low.   |
| GNT3#/GPIO55<br>GNT2#/GPIO53<br>GNT1#/GPIO51 | GNT[3:0]# functionality is not available on Mobile.<br>Mobile: Used as GPIO only<br>Pull-up resistors are not required on these signals.<br>If pull-ups are used, they should be tied to the Vcc3_3power rail.   |
| DF_TVS                                       | DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor.   |
| HAD_DOCK_EN#<br>/GPIO[33]                    | This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33. |
| HDA_SDO                                      | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.  |
| HDA_SYNC                                     | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.  |
| GPIO15                                       | Low (0)<br>Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality<br>High (1)<br>Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality   |

Power Plane

| Power Plane  | Voltage   | Actice Status | Description                                    |
|--|---|---------------|--|
| 5V_S0<br>3D3V_S0<br>1D8V_S0<br>1D5V_S0<br>1D05V_VTT<br>1V_S0<br>0D85V_S0<br>0D75V_S0<br>VCC_CORE<br>VCC GFXCORE<br>1D8V_VGA_S0<br>3D3V_VGA_S0<br>1V_VGA_S0 | 5V<br>3.3V<br>1.8V<br>1.5V<br>1.05V<br>1V<br>0.85V<br>0.75V<br>0.3V to 1.3V<br>0 to 1.25V<br>1.8V<br>3.3V<br>1V | S0            | CPU Core Rail<br>Graphics Core Rail            |
| 5V_USBX_S3<br>1D5V_S3<br>DDR_VREF_S3   | 5V<br>1.5V<br>0.75V   | S3            |  |
| BT+<br>DCBATOUT<br>5V_S5<br>5V_AUX_S5<br>3D3V_S5<br>3D3V_AUX_S5  | 6V-14.1V<br>6V-14.1V<br>5V<br>5V<br>3.3V<br>3.3V  | All S states  | AC Brick Mode only                             |
| 3D3V_LAN_S5  | 3.3V  | WOL_EN        | Legacy WOL                                     |
| 3D3V_AUX_KBC   | 3.3V  | DSW, Sx       | ON for supporting Deep Sleep states            |
| 3D3V_AUX_S5  | 3.3V  | G3, Sx        | Powered by Li Coin Cell in G3 and +V3ALW in Sx |

Chief River Schematic Checklist Rev.0\_72

Sandy & Ivy Bridge Compatibility

| Pin Name                 | Configuration             | Schematic Notes  |
|--------------------------|---------------------------|--|
| DDR3 VREF                | Sandy Bridge + Ivy Bridge | DDR3 VREF, M1 and M3 function are required.  |
|                          | Ivy Bridge                | No change.   |
| PROC_SELECT# &<br>DF_TVS | Sandy Bridge + Ivy Bridge | Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH VccDFTERM rail.         |
|                          | Ivy Bridge                | No change.   |
| VCCIO_SEL                | Sandy Bridge + Ivy Bridge | The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a need for a separate VR for the processor at 1.0 V and the PCH at 1.05 V. A single VR may be shared for both. |
|                          | Ivy Bridge                | No change.   |
| VCCSA_VID[0:1]           | Sandy Bridge + Ivy Bridge | VCCSA[0:1] are the select pin of VCCSA's power control.  |
|                          | Ivy Bridge                | No change.   |

Processor Strapping

| Pin Name | Strap Description                   | Configuration (Default value for each bit is 1 unless specified otherwise)  | Default Value | POP Value |
|----------|-------------------------------------|---|---------------|-----------|
| CFG[2]   | PCI-Express Static Lane Reversal    | 1: Normal Operation.<br>0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...  | 1             | 0         |
| CFG[4]   |                                     | 1: Disabled - No Physical Display Port attached to Embedded DisplayPort.<br>0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port | 1             | 1         |
| CFG[6:5] | PCI-Express Port Bifurcation Straps | 11: 1x16 PCI Express<br>10: 2 x8 - PCI Express<br>01: Reserved<br>00: 1x8, 2x4 PCI Express  | 11            | 10        |

USB Table

| Pair | Device                         |
|------|--------------------------------|
| 0    | USB3.0 port1, with Power Share |
| 1    | USB3.0 port2, debug port       |
| 2    | NC                             |
| 3    | NC                             |
| 4    | Touch Panel                    |
| 5    | NC                             |
| 6    | NC                             |
| 7    | NC                             |
| 8    | WWAN                           |
| 9    | NC                             |
| 10   | Card reader                    |
| 11   | WLAN                           |
| 12   | CAMERA                         |
| 13   | NC                             |

PCIE Table

| PCIE |             |
|------|-------------|
| Lane | Device      |
| 1    | NC          |
| 2    | NC          |
| 3    | NC          |
| 4    | WLAN        |
| 5    | NC          |
| 6    | Onboard LAN |
| 7    | NC          |
| 8    | NC          |

SATA Table

| SATA |        |
|------|--------|
| Pair | Device |
| 0    | HDD1   |
| 1    | mSATA  |
| 2    | NC     |
| 3    | NC     |
| 4    | ODD    |
| 5    | NC     |

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SSID = CPU

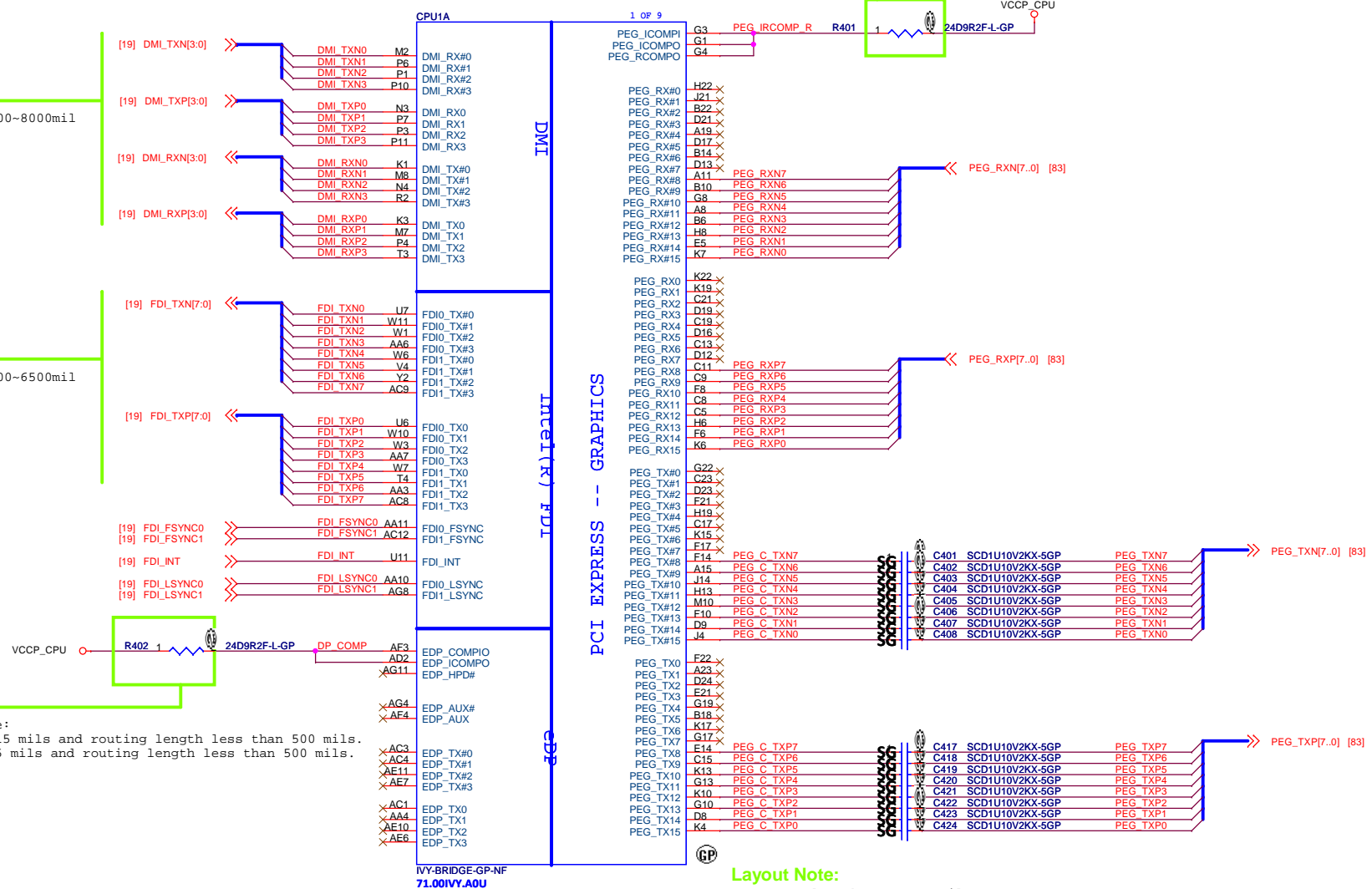
Layout Note:  
DMI trace length 2000~8000mil

Layout Note:  
FDI trace length 2000~6500mil

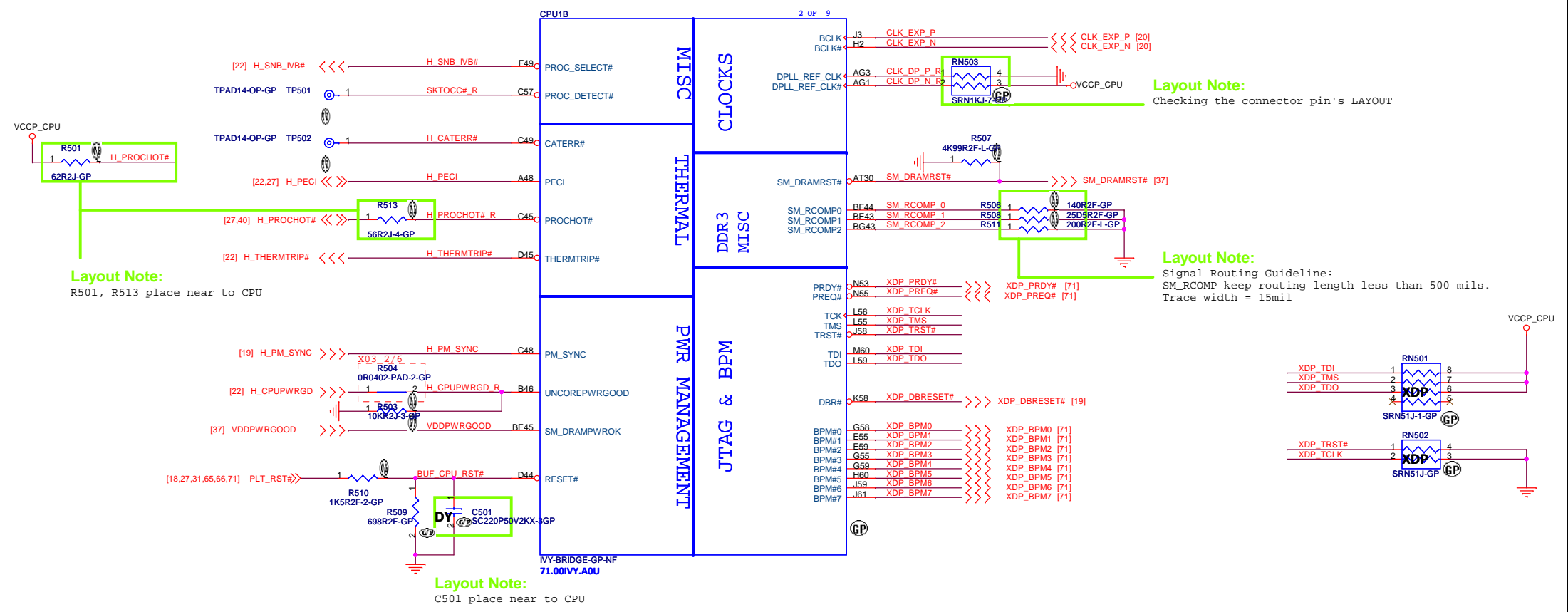
Layout Note:  
Signal Routing Guideline:  
EDP\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
EDP\_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:  
PEG trace length 1500~9000mil

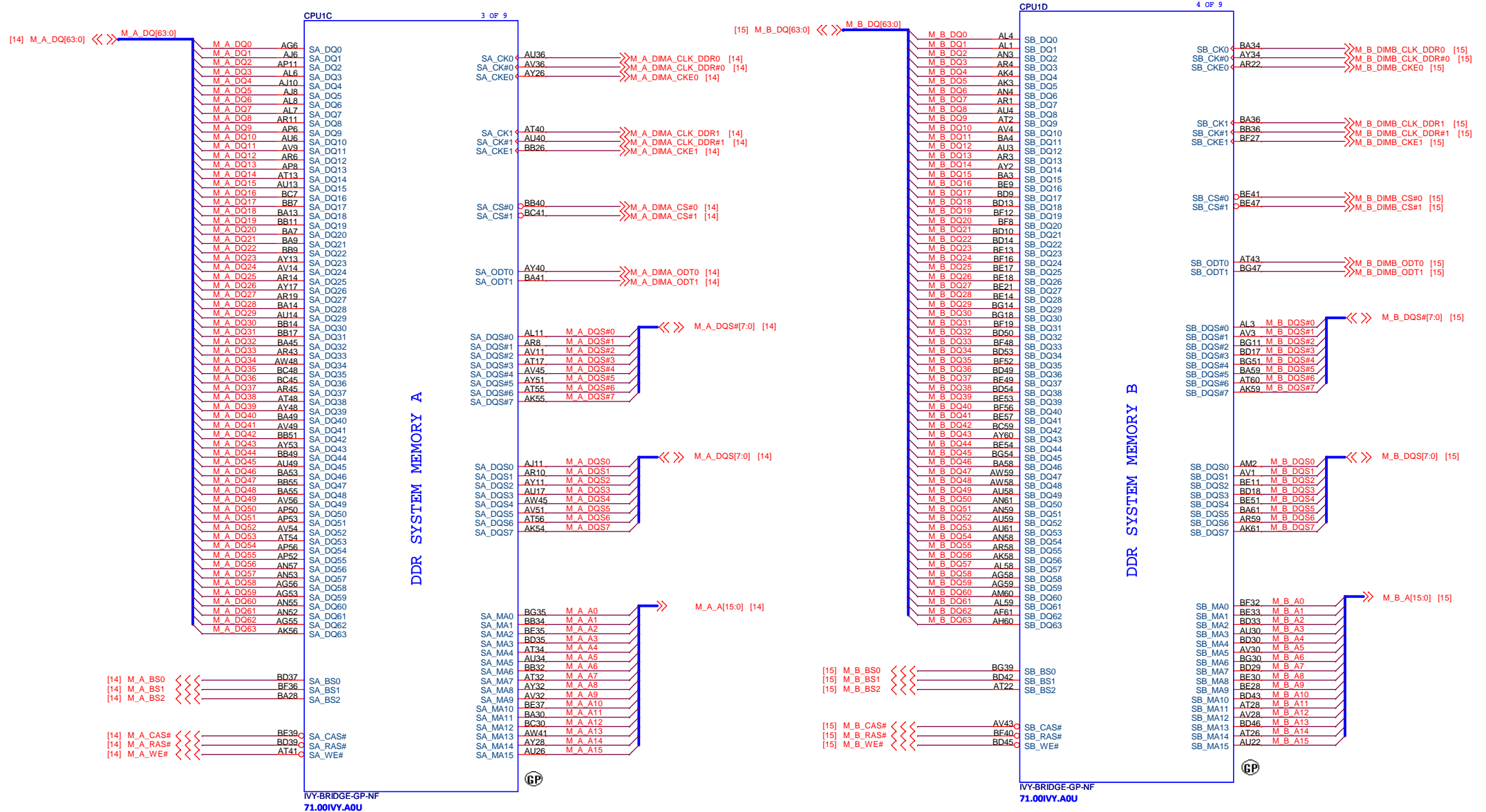
Layout Note:  
Signal Routing Guideline:  
PEG\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
PEG\_ICOMPI & PEG\_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



SSID = CPU



SSID = CPU



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| Title | Author | Year | Journal | Volume | Page |
|-------|--------|------|---------|--------|------|
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**CPU (DDR)**Size  
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| Document Number |
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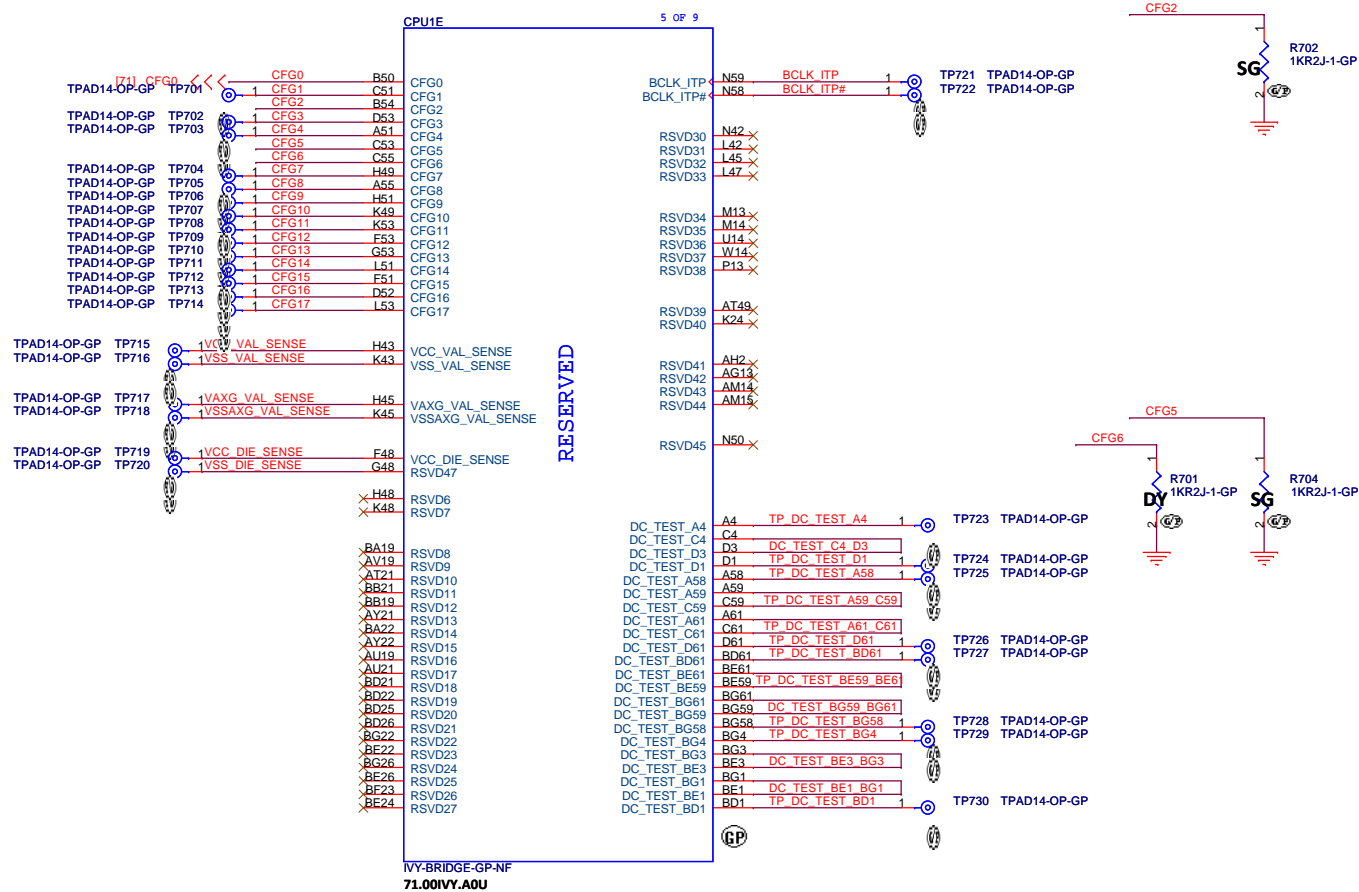
Date \_\_\_\_\_

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SSID = CPU



|                          |   |
|--------------------------|---|
| PEG Static Lane Reversal |   |
| CFG[2]                   | 1: Normal Operation; Lane #<br>definition matches socket pin map definition |
|                          | 0: Lane Reversed  |

| Display Port Presence Strap |   |
|-----------------------------|---|
| CFG[4]                      | 1: Disabled; No Physical Display Port attached to Embedded Display Port               |
|                             | 0: Enabled; An external Display Port device is connected to the Embedded Display Port |

| PCIe Port Bifurcation Straps |                          |
|------------------------------|--------------------------|
| CFG[6:5]                     | 11: 1x16 PCI Express     |
|                              | 10: 2 x8 - PCI Express   |
|                              | 01: Reserved             |
|                              | 00: 1x8, 2x4 PCI Express |



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***CPU (RESERVED)***

Size

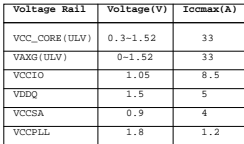
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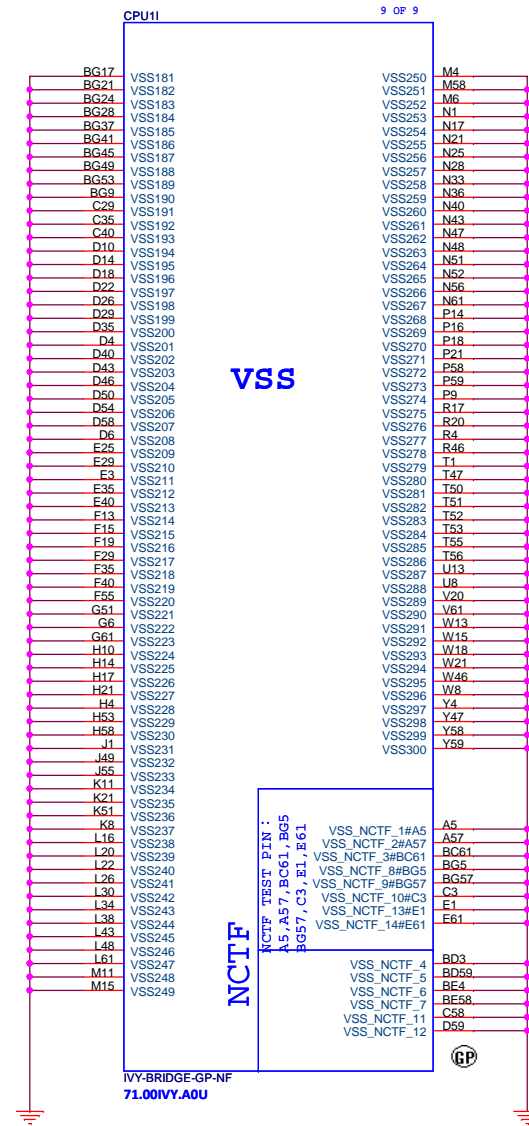
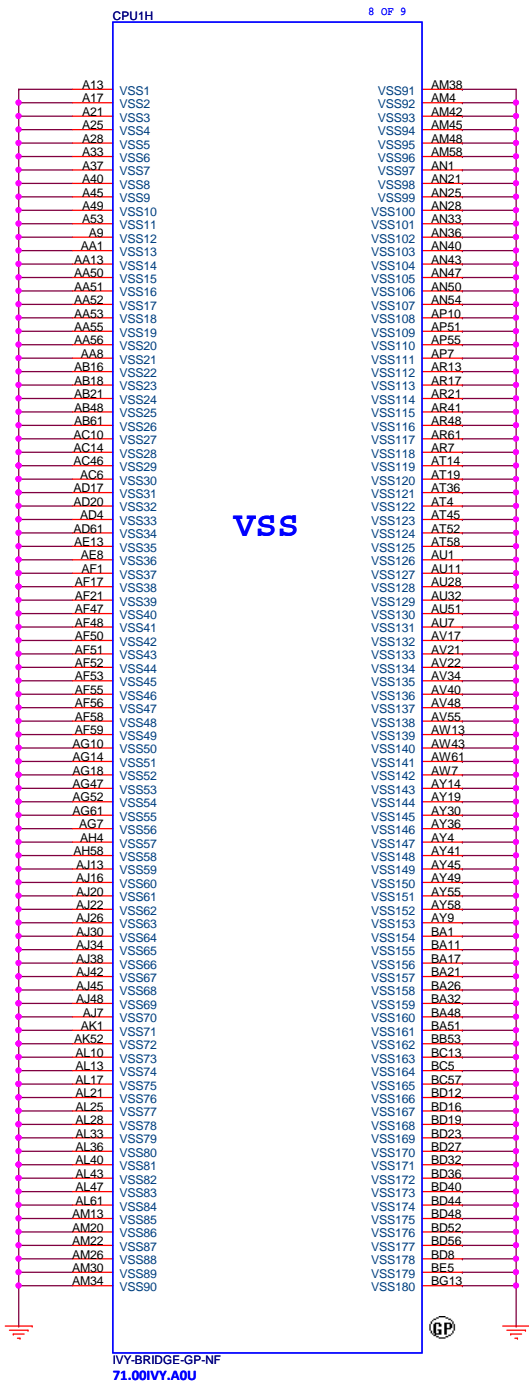
- Layout Note:
  1. PH/PL resistors place close CPU
  2. SENSE signal recommend differential routing

- Layout Note:
  1. PH/PL resistors place close CPU
  2. SENSE signal recommend differential routing





SSID = CPU



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Title: **CPU (VSS)**

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***XDP***

Size

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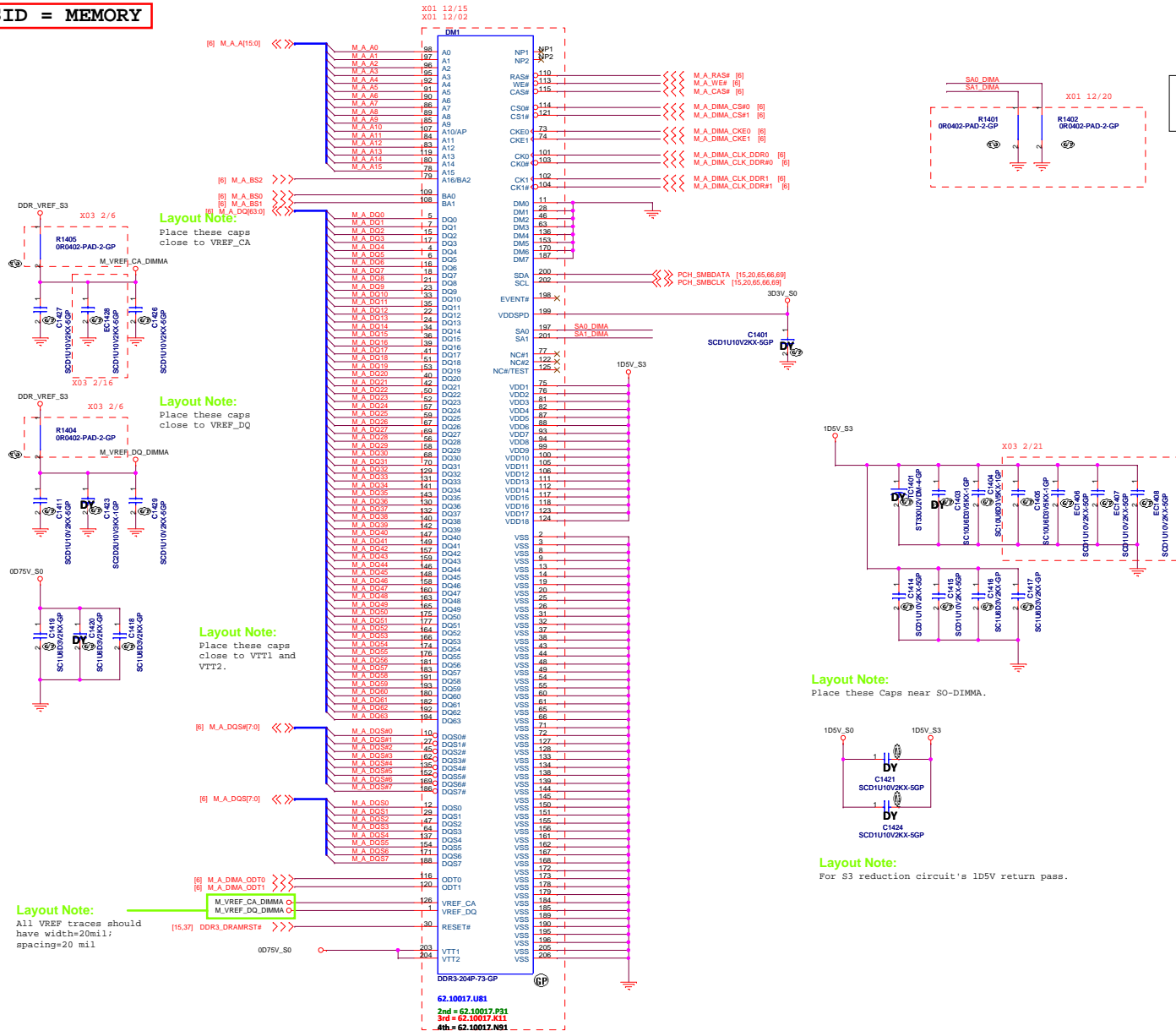
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**A00**

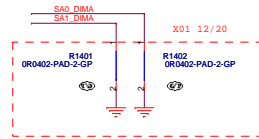
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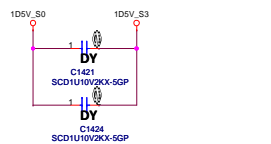
## SSID = MEMORY



**Note:**  
SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30



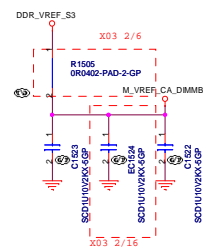
**Layout Note:**  
Place these Caps near SO-DIMMA.



**Layout Note:**  
For S3 reduction circuit's 1D5V return pass.

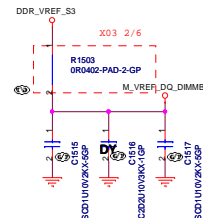


## SSID = MEMORY



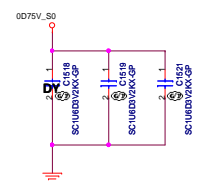
**Layout Note:**

Place these caps close to VREF\_CAP



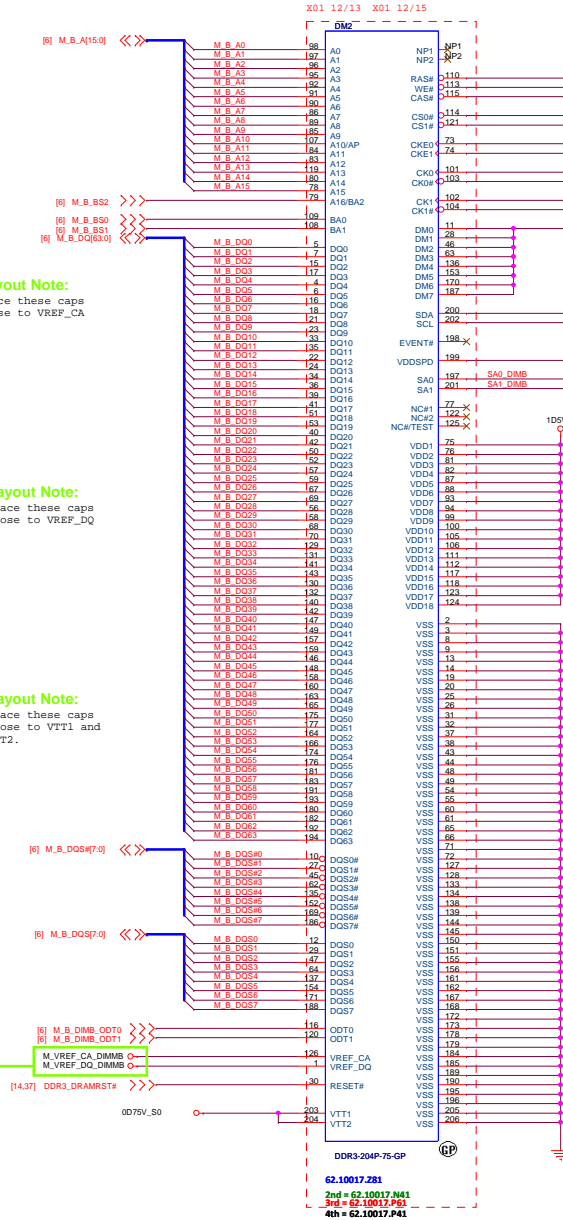
### Layout Note

**Layout Note:**  
Place these caps close to VREF<sub>1</sub>.



### Layout Note

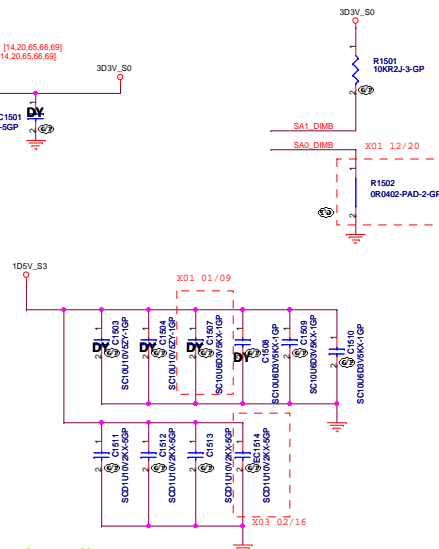
**Layout Note.**  
Place these caps close to VTT1 and VTT2.



**Layout Note:**

Place these Caps near SO-DIMMA

**Note:**  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34



**Layout Note:**

Place these Caps near SO-DIMMA



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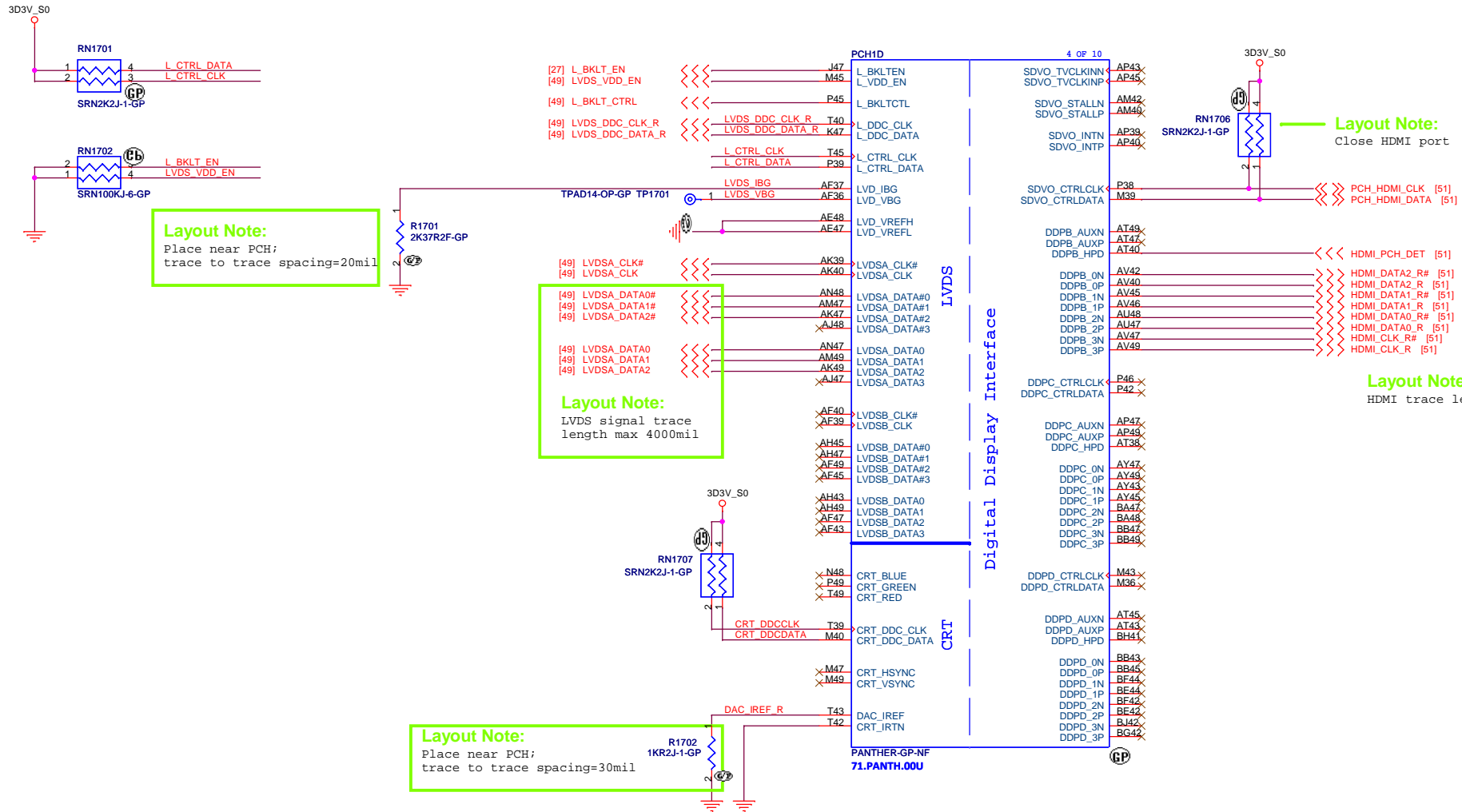
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**Reserved**



# SSID = PCH



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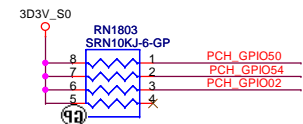
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|       |                        |            |                           |        |
|-------|------------------------|------------|---------------------------|--------|
| Title |                        |            | <b>PCH (LVDS/CRT/DDI)</b> |        |
| Size  | Document Number        | Rev        |                           |        |
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**SSID = PCH**

## USB3.0/2.0 Mapping Table

| USB 3.0 Port | USB 2.0 port |
|--------------|--------------|
| Port 1       | Port 0       |
| Port 2       | Port 1       |
| Port 3       | Port 2       |
| Port 4       | Port 3       |



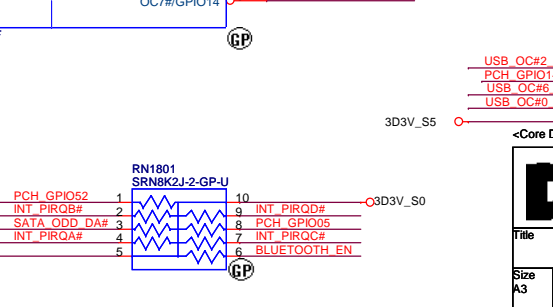
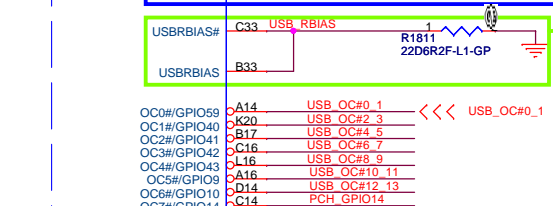
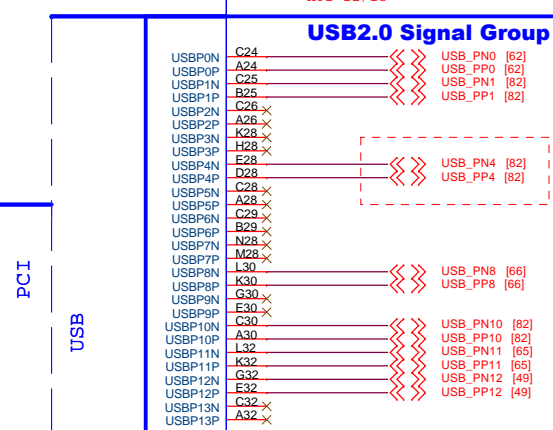
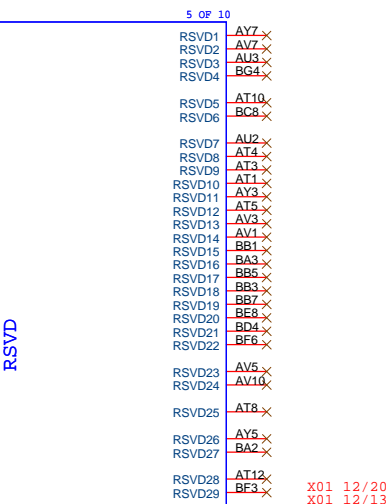
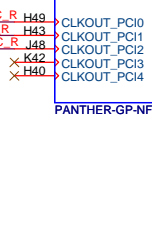
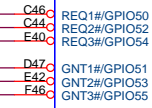
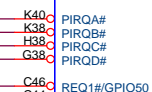
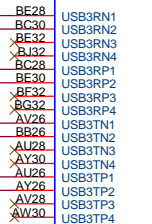
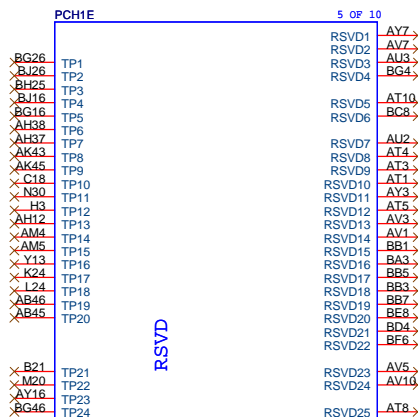
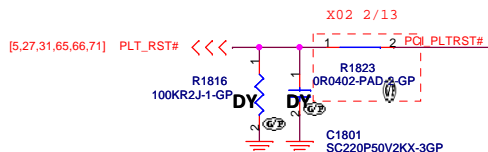
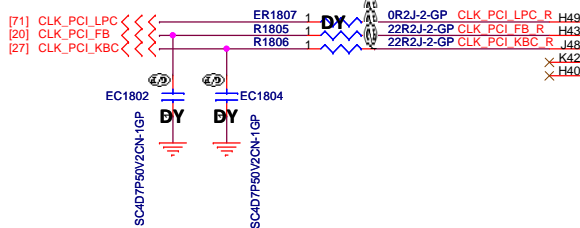
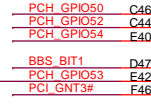
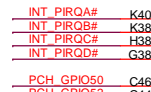
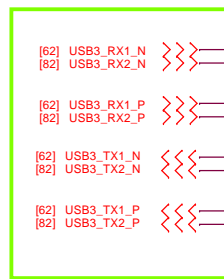
| Boot Bios Strap |                |                    |
|-----------------|----------------|--------------------|
| GNT1#/GPIO51    | SATA1GF/GPIO19 | Boot BIOS Location |
| 0               | 0              | LPC                |
| 0               | 1              | Reserved           |
| 1               | 0              | Reserved           |
| 1               | 1              | SPI(Default)       |



|                          |  |
|--------------------------|--|
| A16 Swap Override jumper |  |
| PCI_GNT#3                | Low = A16 swap override/Top-Block<br>Swap Override enabled<br>High = Default |

**Layout Note:**

Trace Length :  
PCH ~~9000mil~~Cap~~1000mil~~CONN



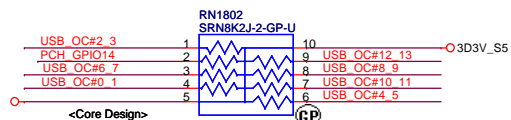
## USB Table

| Pair | Device                         |
|------|--------------------------------|
| 0    | USB3.0 port1, with Power Share |
| 1    | USB3.0 port2                   |
| 2    | NC                             |
| 3    | NC                             |
| 4    | Touch Panel                    |
| 5    | NC                             |
| 6    | NC                             |
| 7    | NC                             |
| 8    | WWAN                           |
| 9    | NC                             |
| 10   | Card reader                    |
| 11   | WLAN                           |
| 12   | CAMERA                         |
| 13   | NC                             |

1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.

→ **Layout Note:**

1. USBBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil

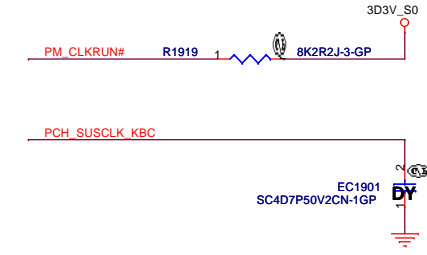
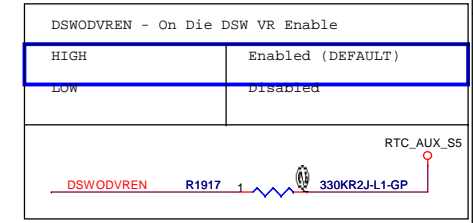
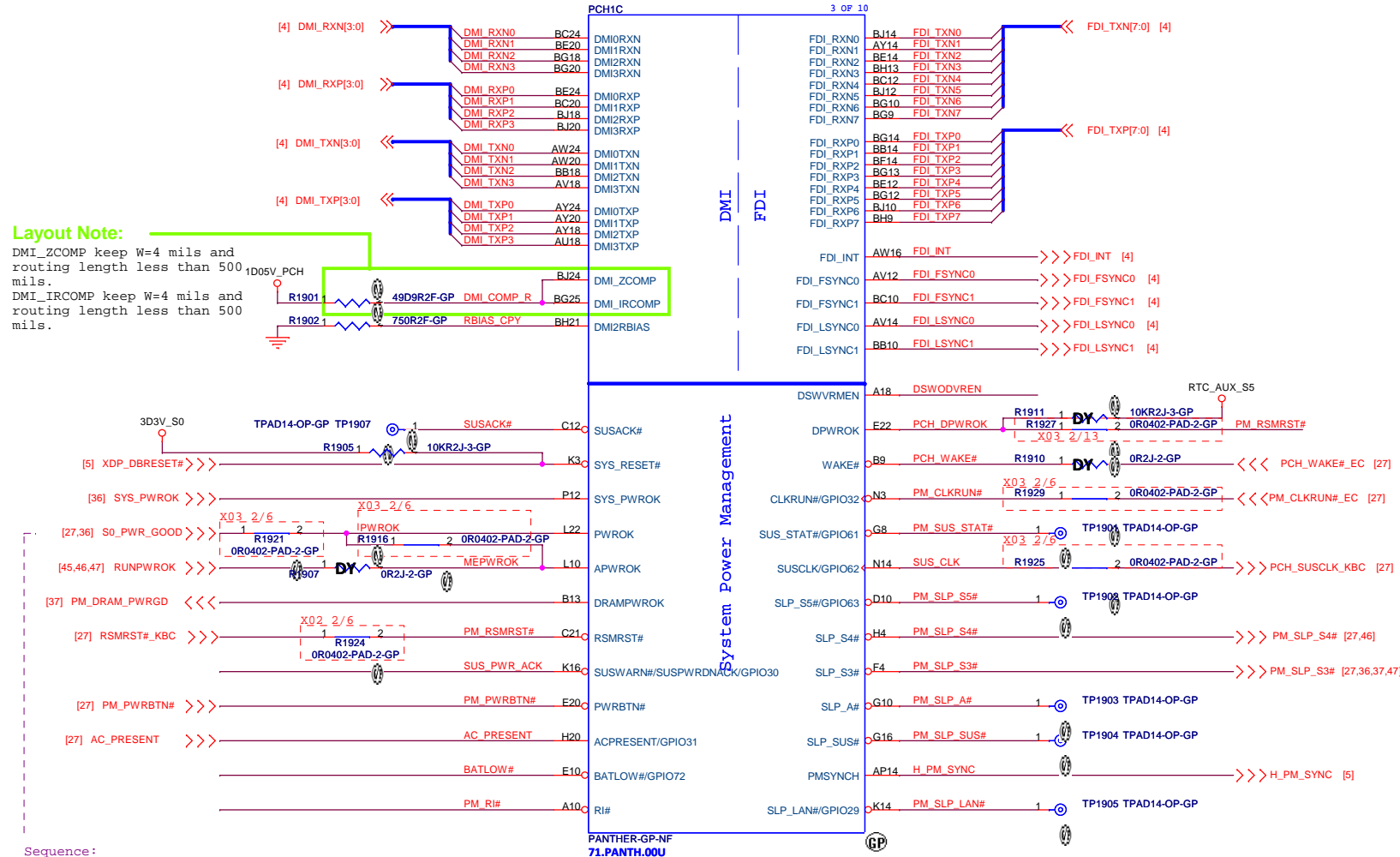


|       |                        |  |  |                            |    |    |     |
|-------|------------------------|--|--|----------------------------|----|----|-----|
| Title |                        |  |  | <b>PCH (PCI/USB/NVRAM)</b> |    |    |     |
| Size  | Document Number        |  |  |                            |    |    | Rev |
| A3    | <b>BMW Z4 DIS</b>      |  |  |                            |    |    | A00 |
| Date: | Friday, March 30, 2012 |  |  | Sheet                      | 18 | of | 105 |

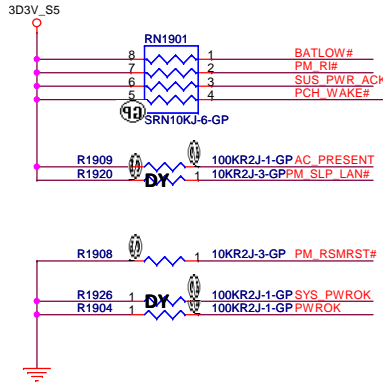
# SSID = PCH

## Layout Note:

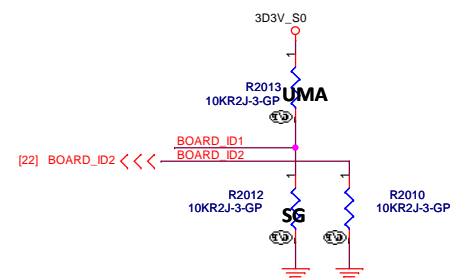
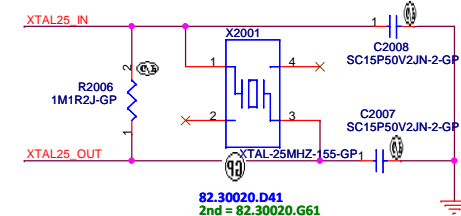
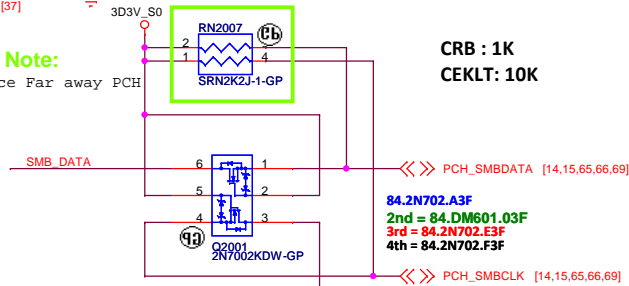
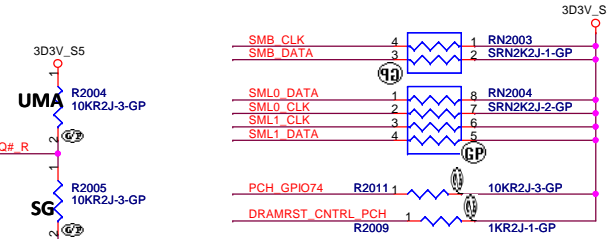
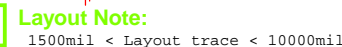
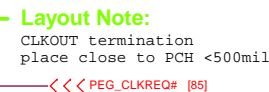
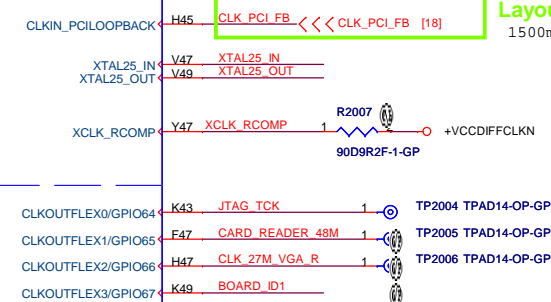
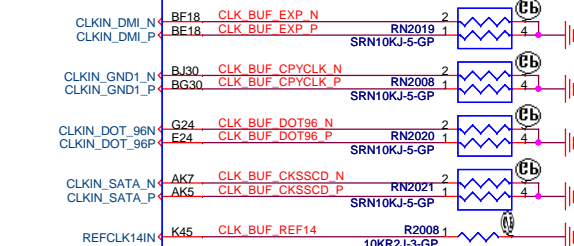
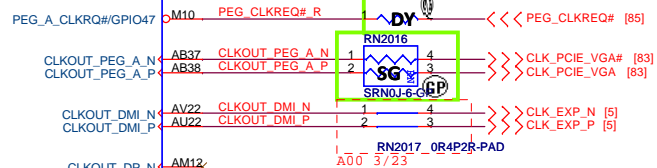
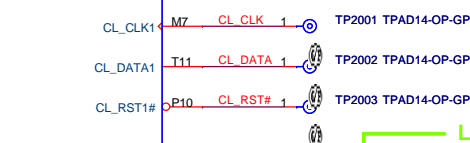
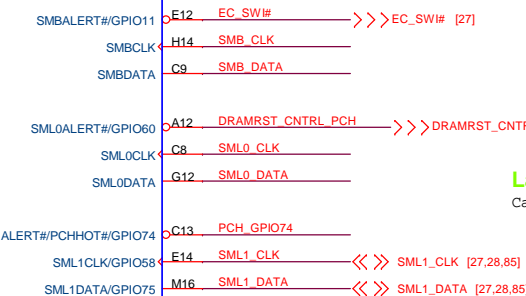
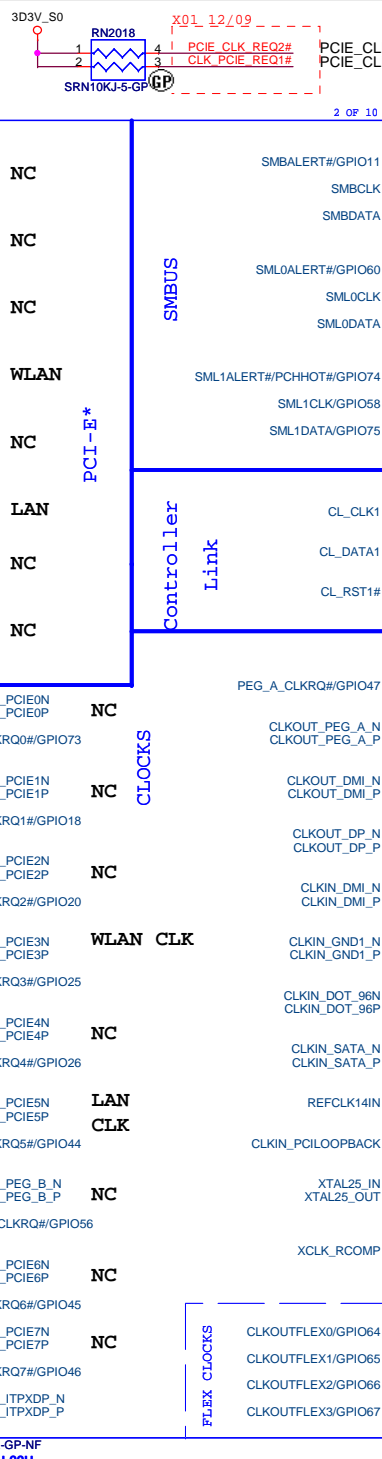
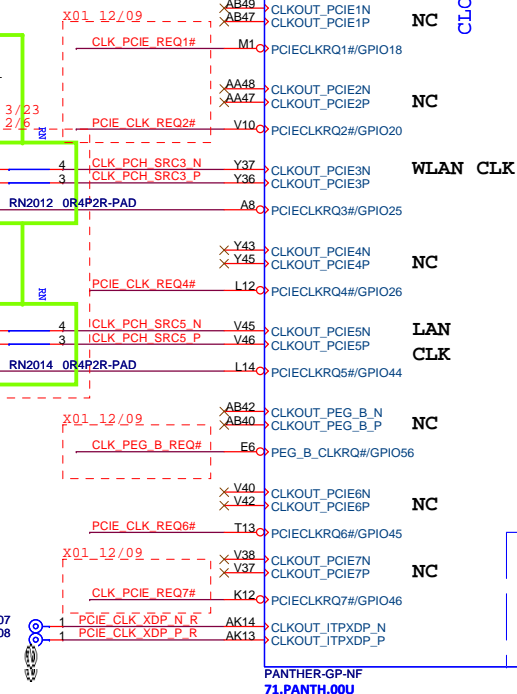
DMI\_ZCOMP keep W=4 mils and routing length less than 500 mils.  
DMI\_IRCOMP keep W=4 mils and routing length less than 500 mils.



Sequence:  
S0\_PWR\_GOOD after PM\_SLP\_S3# delay 200 ms



S5 power rail CLKREQ#:  
PCIECLKRQ[0]#  
PCIECLKRQ[7:3]#



| BIOS UMA/DIS Strap pin |           |           |
|------------------------|-----------|-----------|
|                        | BOARD_ID1 | BOARD_ID2 |
| PX(AMD)                | 0         | 0         |
| DIS                    | 0         | 1         |
| UMA                    | 1         | 0         |
| Optimus(NV)            | 1         | 1         |

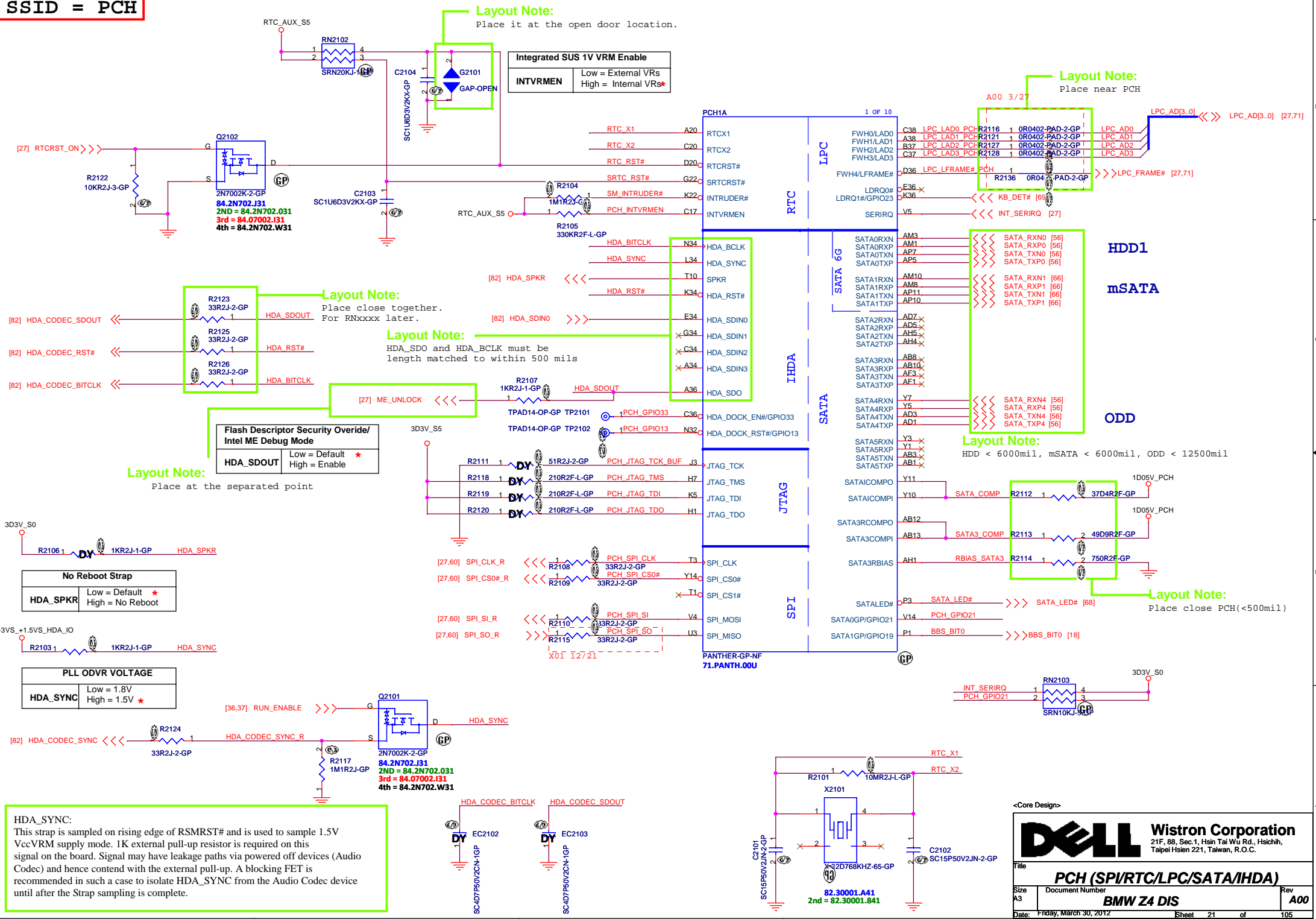


|       |                                   |
|-------|-----------------------------------|
| Title | <b>PCH (PCI-E/SMBUS/CLOCK/CL)</b> |
|-------|-----------------------------------|

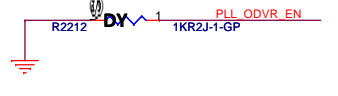
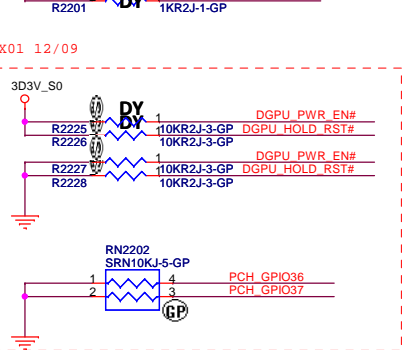
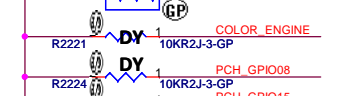
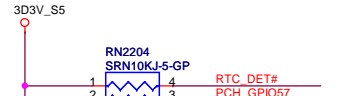
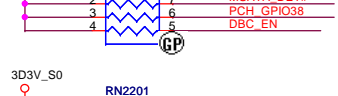
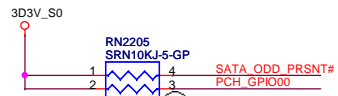
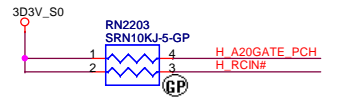
|            |                                      |                   |
|------------|--------------------------------------|-------------------|
| Size<br>A3 | Document Number<br><b>BMW Z4 DIS</b> | Rev<br><b>A00</b> |
|------------|--------------------------------------|-------------------|

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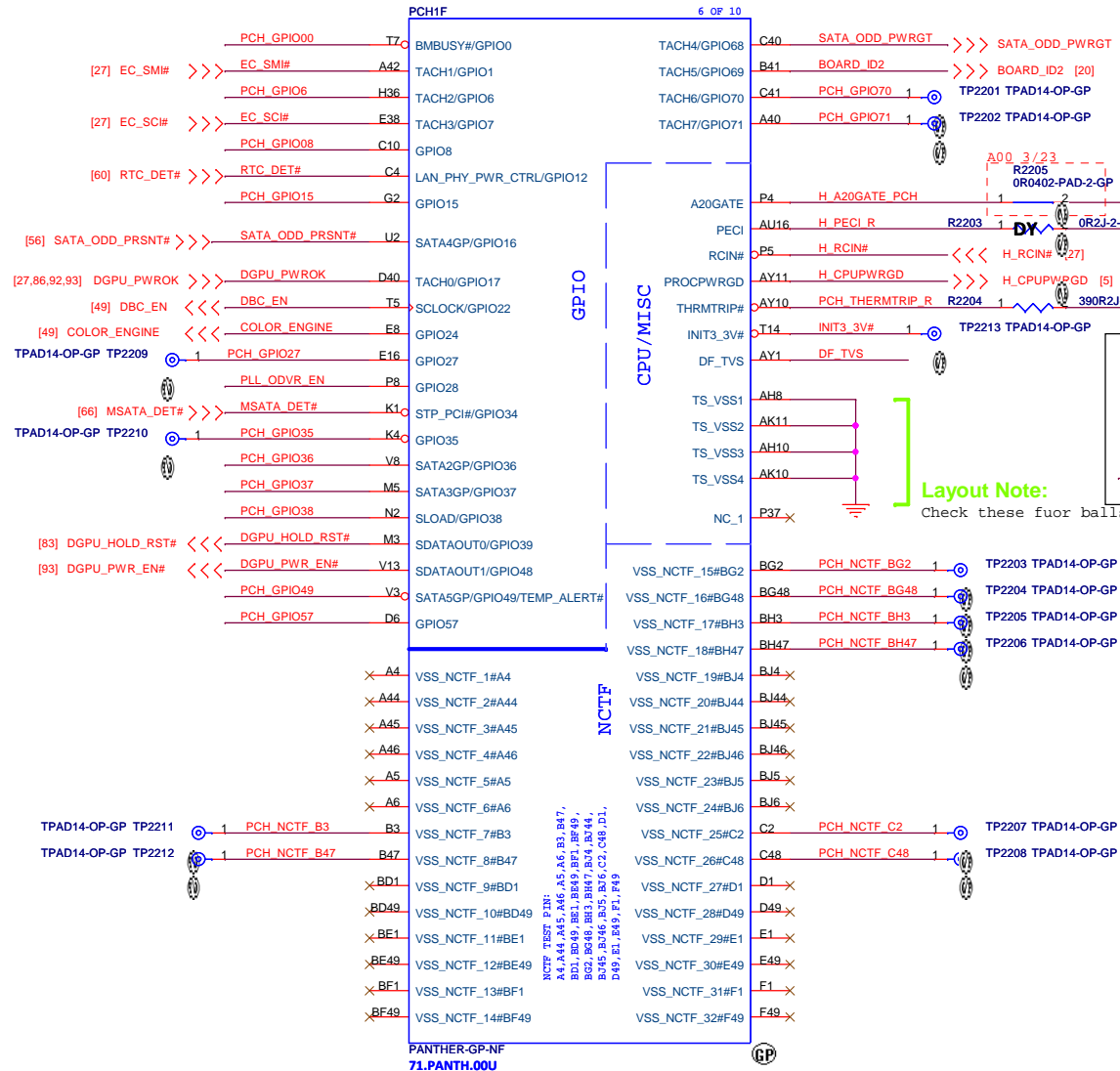
SSID = PCH



# SSID = PCH



|                         |  |
|-------------------------|--|
| PLL ON DIE VR ENABLE    |  |
| GPIO28<br>(PLL_ODVR_EN) | Weakly internal pull up 20k.<br>High - Enable<br>LOW - Disable |



Layout Note:

Check these four balls are connected firstly, then to GND

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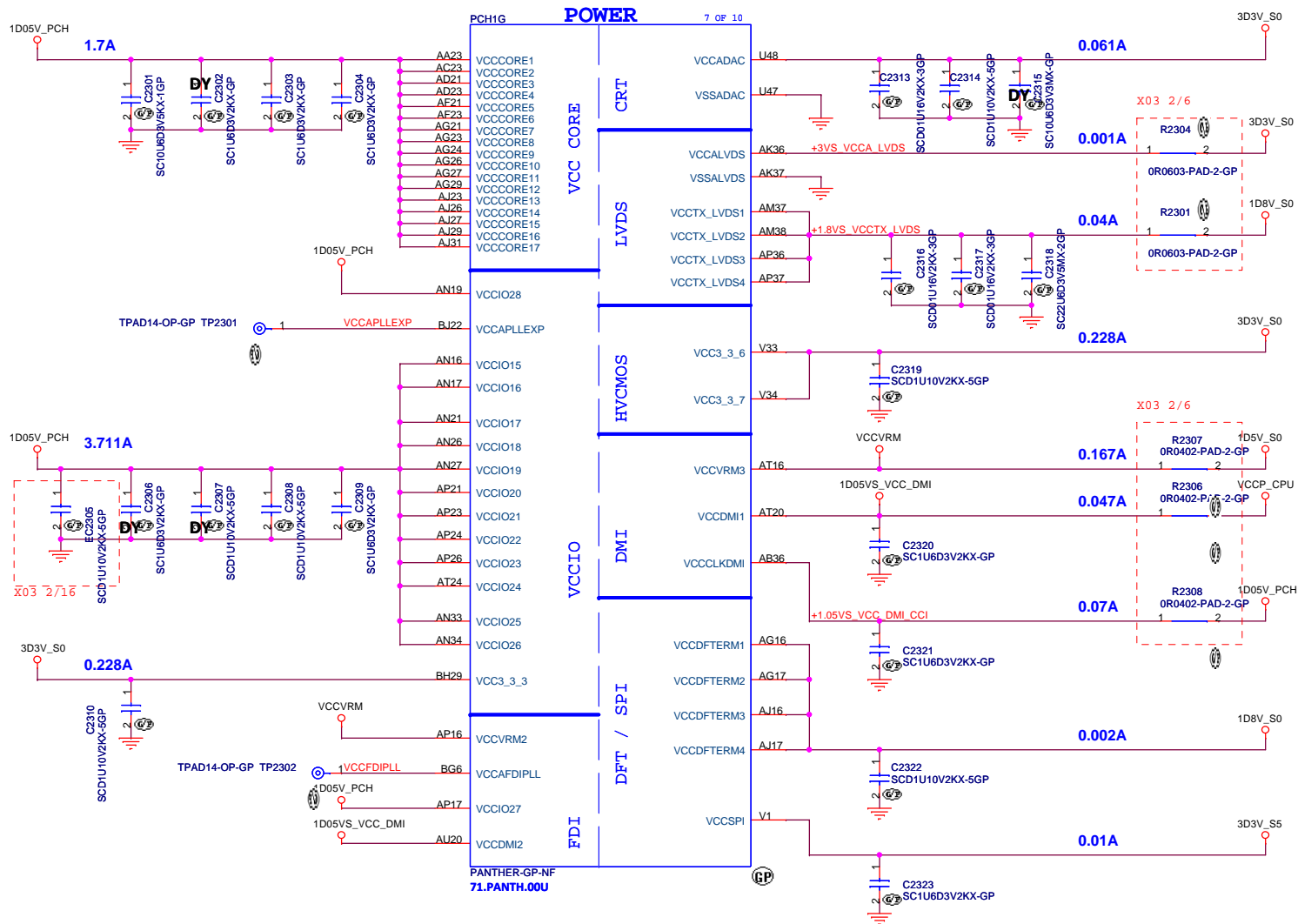
Title: **PCH (GPIO/CPU)**

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SSID = PCH



| Voltage Rail | Voltage(V) | Iccmax(A) |
|--------------|------------|-----------|
| V_PROC_IO    | 1.05       | 0.001     |
| V5REF        | 5          | 0.001     |
| V5REF_Sus    | 5          | 0.001     |
| Vcc3_3       | 3.3        | 0.228     |
| VccADAC      | 3.3        | 0.063     |
| VccADPLLA    | 1.05       | 0.08      |
| VccADPLLB    | 1.05       | 0.08      |
| VccCore      | 1.05       | 1.7       |
| VccDMI       | 1.1        | 0.047     |
| VccIO        | 1.05       | 3.711     |
| VccASW       | 1.05       | 0.903     |
| VccSPI       | 3.3        | 0.01      |
| VccDSW3_3    | 3.3        | 0.001     |
| VccDFTERM    | 1.8        | 0.002     |
| VccRTC       | 3.3        | 6uA       |
| VccSus3_3    | 3.3        | 0.095     |
| VccSusHDA    | 3.3        | 0.01      |
| VccVRM       | 1.5        | 0.167     |
| VccClkDMI    | 1.05       | 0.07      |
| VccSSC       | 1.05       | 0.095     |
| VccDIFFCLKN  | 1.05       | 0.055     |
| VccALVDS     | 3.3        | 0.001     |
| VccTX_LVDS   | 1.8        | 0.04      |

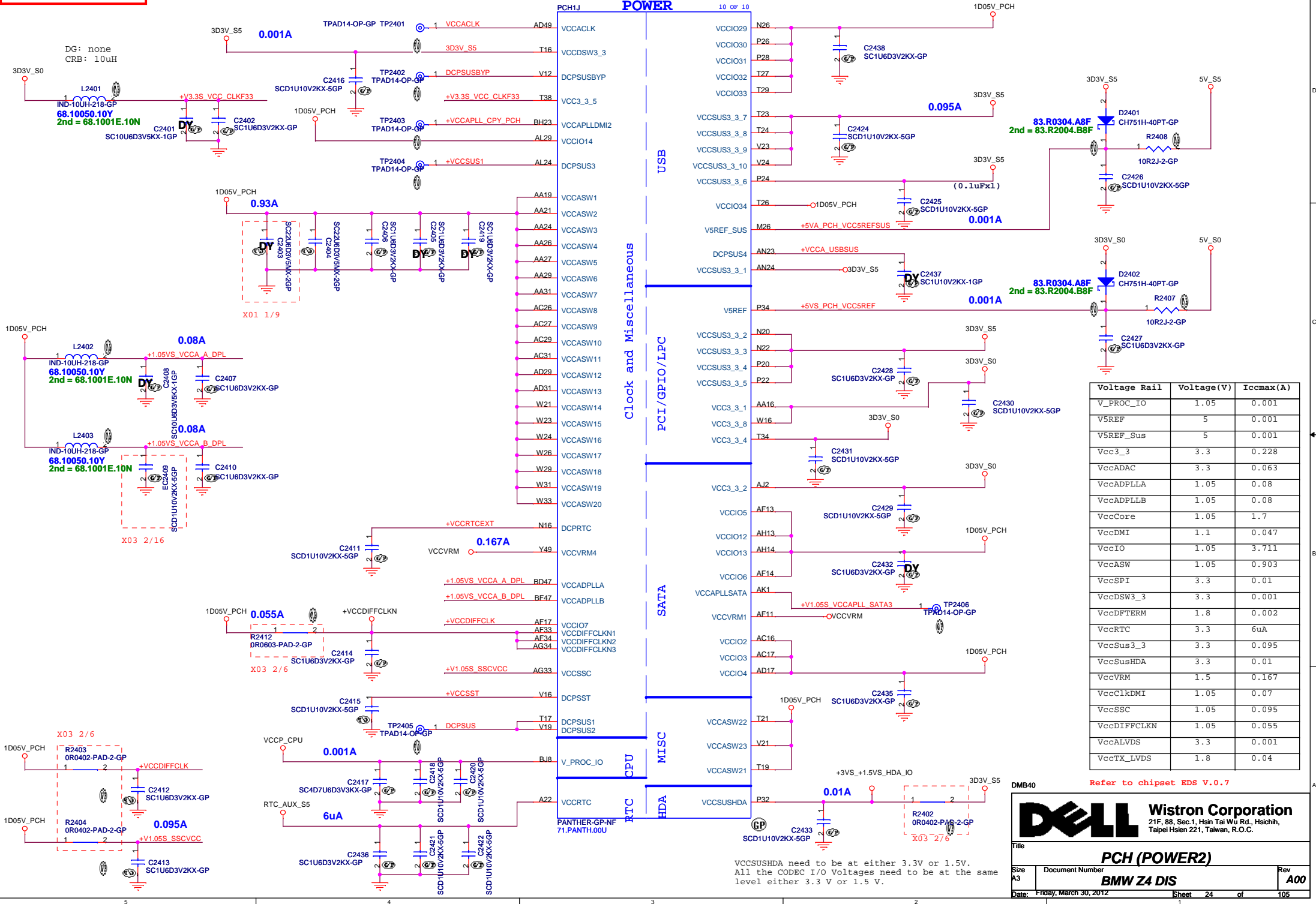
Refer to chipset EDS V.0.7

<Core Design>



|                     |                        |       |    |            |
|---------------------|------------------------|-------|----|------------|
| Title               |                        |       |    |            |
| <b>PCH (POWER1)</b> |                        |       |    |            |
| Size                | Document Number        |       |    | Rev        |
| A3                  | <b>BMW Z4 DIS</b>      |       |    | <b>A00</b> |
| Date:               | Friday, March 30, 2012 | Sheet | 23 | of 105     |

# SSID = PCH



Refer to chipset EDS V.0.7

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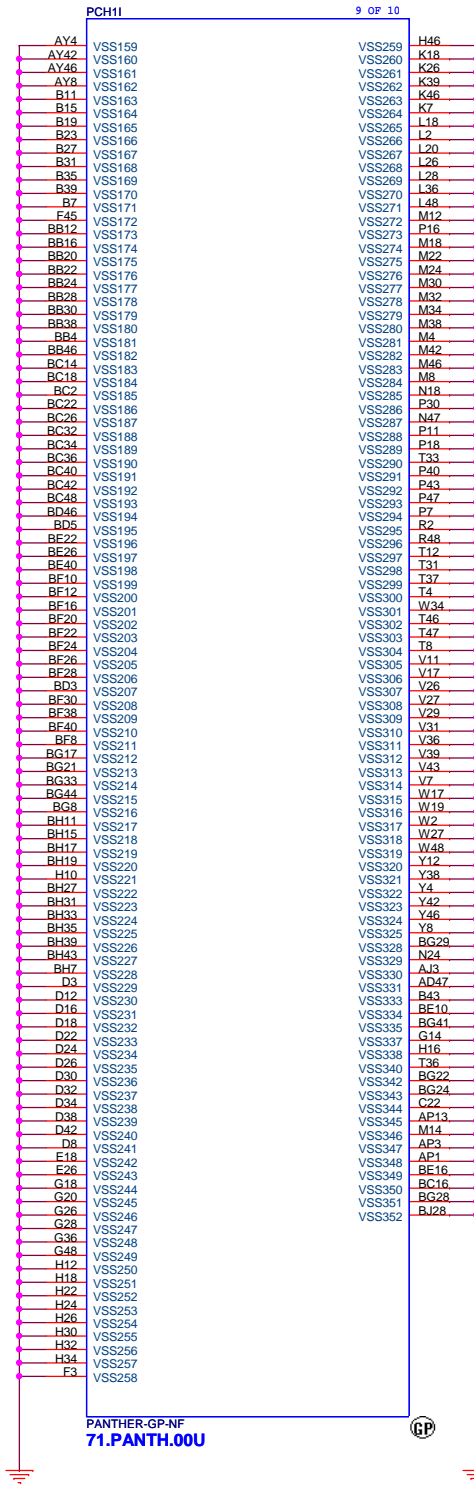
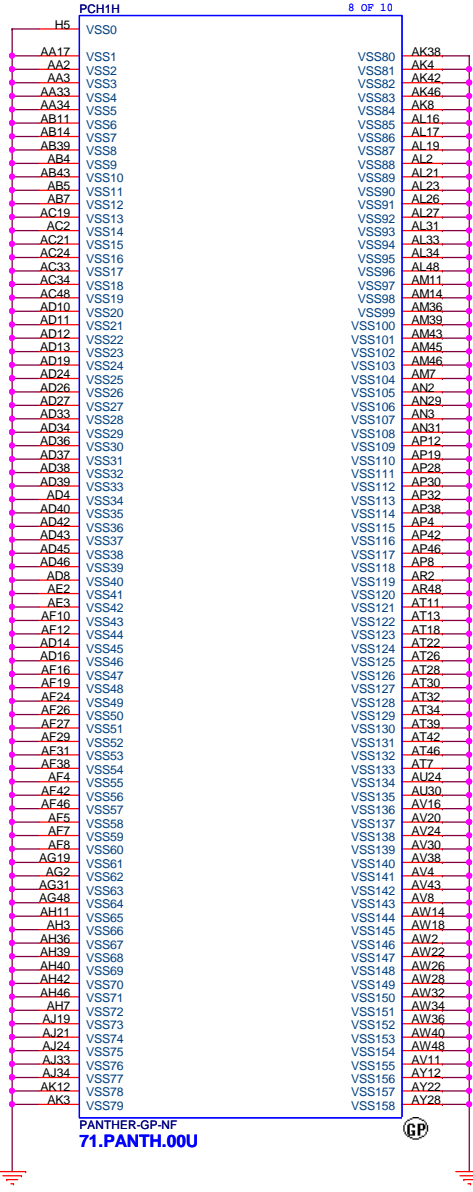
Title: **PCH (POWER2)**

Size A3 Document Number **BMW Z4 DIS** Rev **A00**

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SSID = PCH



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Title **PCH (VSS)**

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Title

**Reserved**

Size  
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Document Number  
**BMW Z4 DIS**

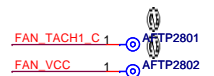
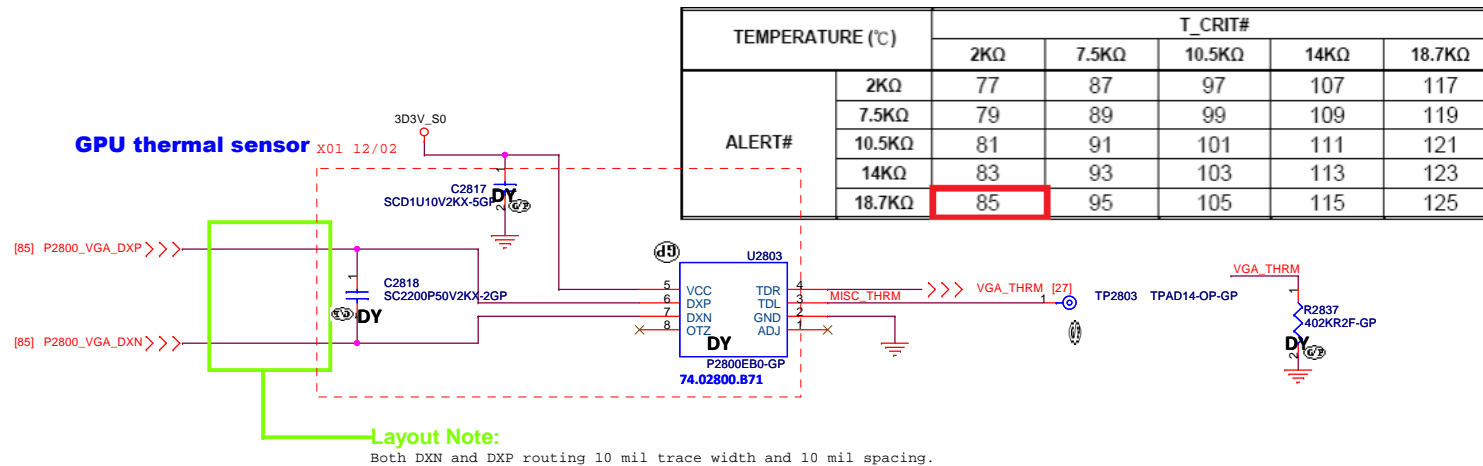
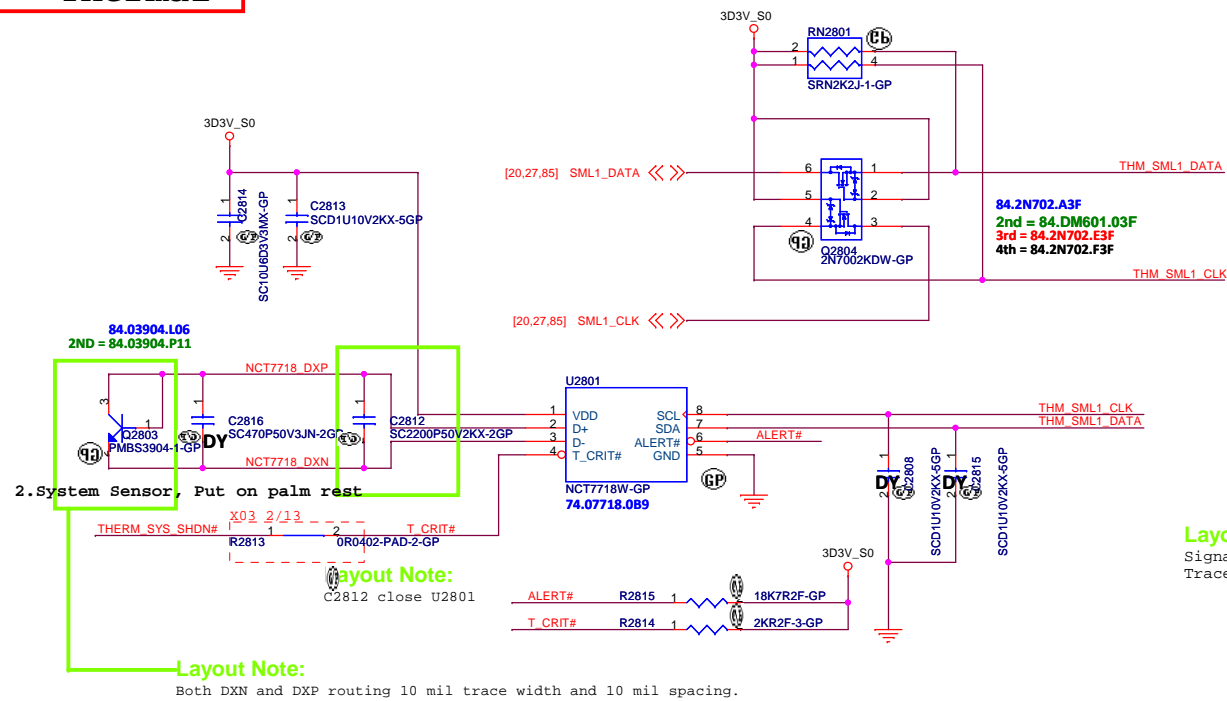
Date: Friday, March 30, 2012

Rev  
**A00**

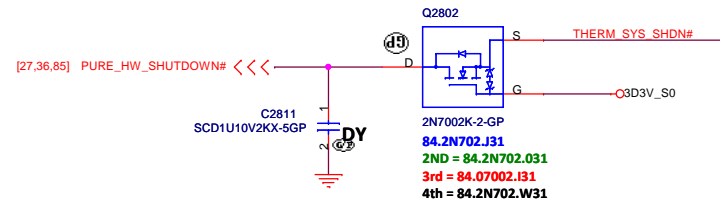
Sheet 26 of 105



SSID = Thermal




| Thermal Sensor |           |
|----------------|-----------|
| Adj            | Temp. (C) |
| Pull high      | 95        |
| Pull low       | 90        |
| Floating       | 85        |



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|   |                                      |   |                   |
|---|--------------------------------------|---|-------------------|
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| Title   |                                      |   |                   |
| <b>Reserved</b>   |                                      |   |                   |
| Size<br>A3  | Document Number<br><b>BMW Z4 DIS</b> |   | Rev<br><b>A00</b> |
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Size  
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Document Number  
**BMW Z4 DIS**

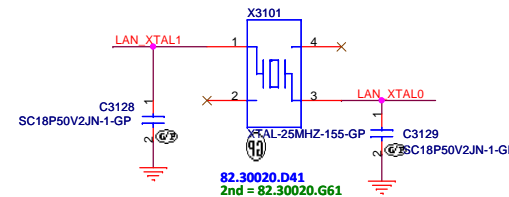
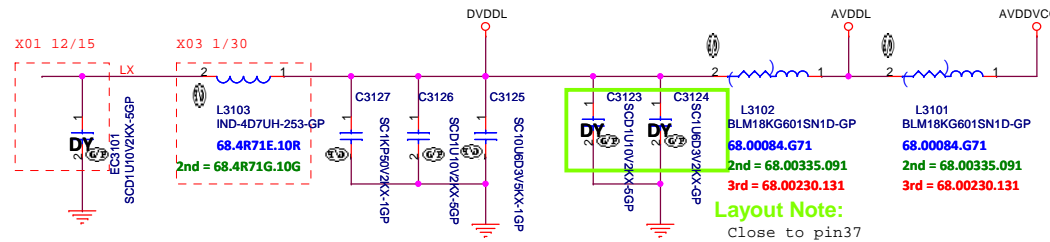
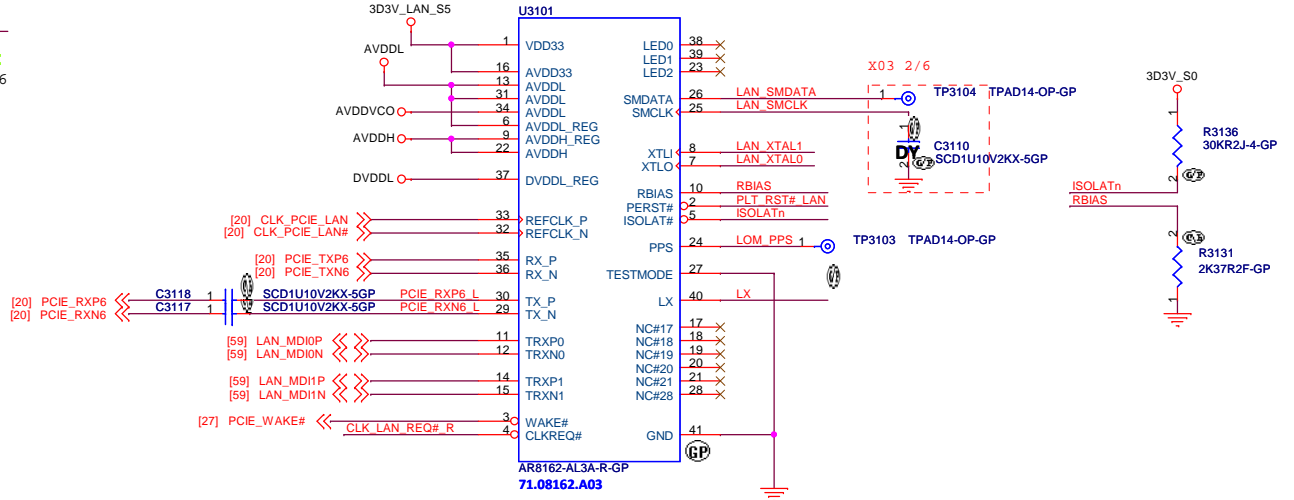
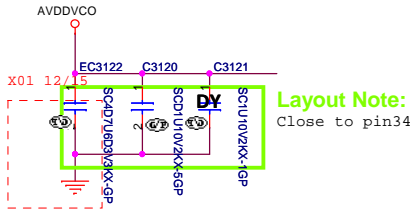
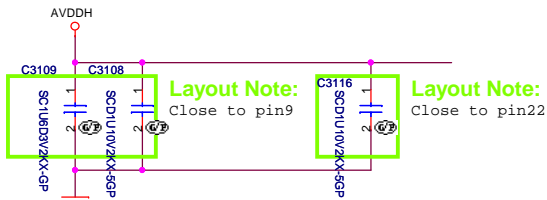
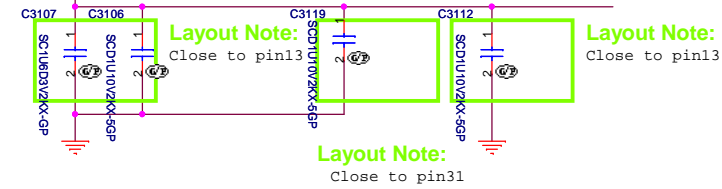
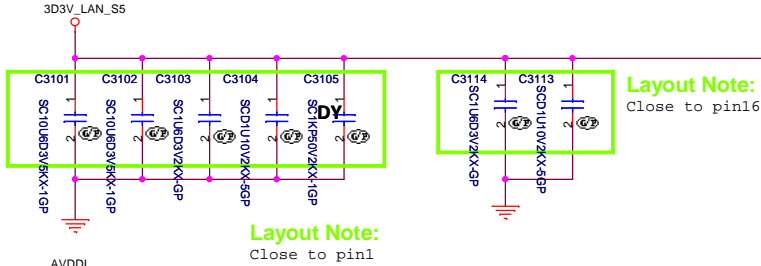
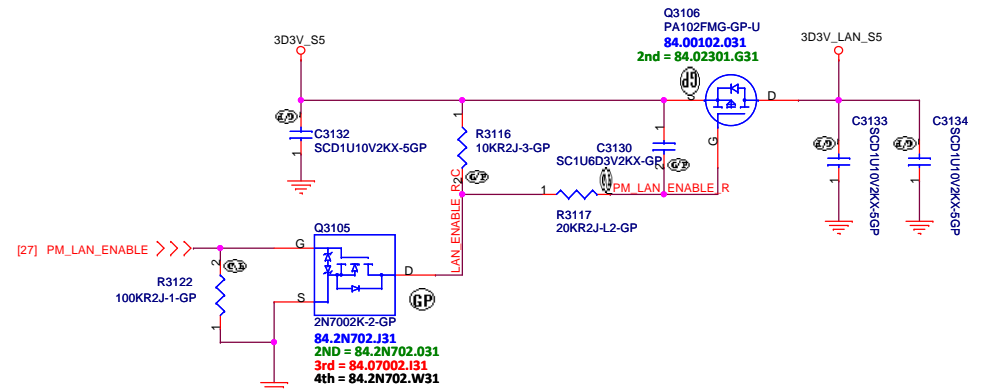
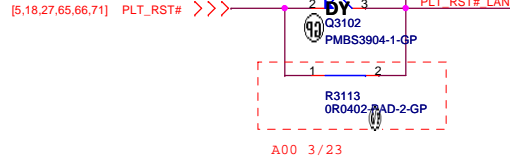
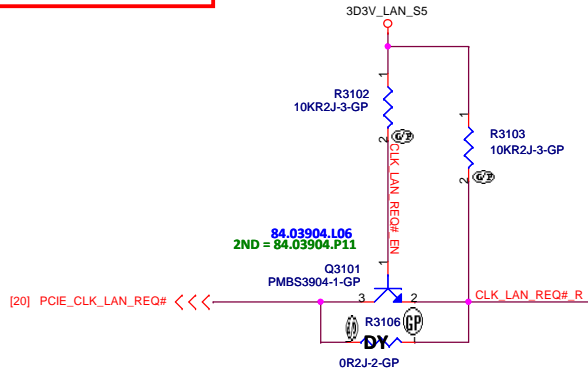
Date: Friday, March 30, 2012

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**SSID = LOM**



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|   |                                      |   |                   |
|---|--------------------------------------|---|-------------------|
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| Title   |                                      |   |                   |
| <b>Reserved</b>   |                                      |   |                   |
| Size<br>A3  | Document Number<br><b>BMW Z4 DIS</b> |   | Rev<br><b>A00</b> |
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**Reserved**

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**Reserved**

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Title

Size  
A3

Document Number  
**BMW Z4 DIS**

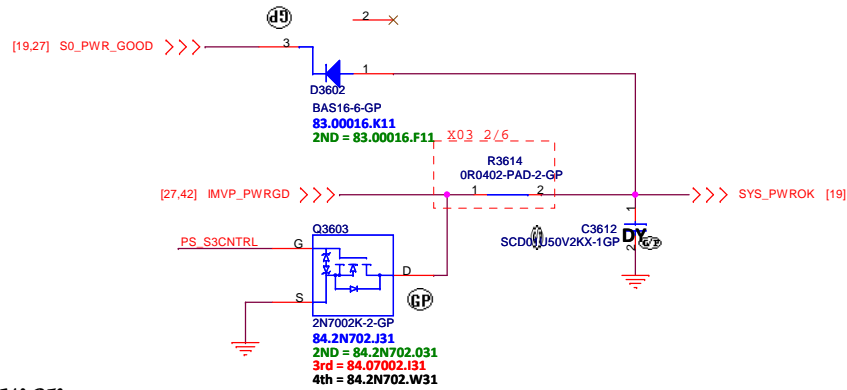
Date: Friday, March 30, 2012

Rev  
**A00**

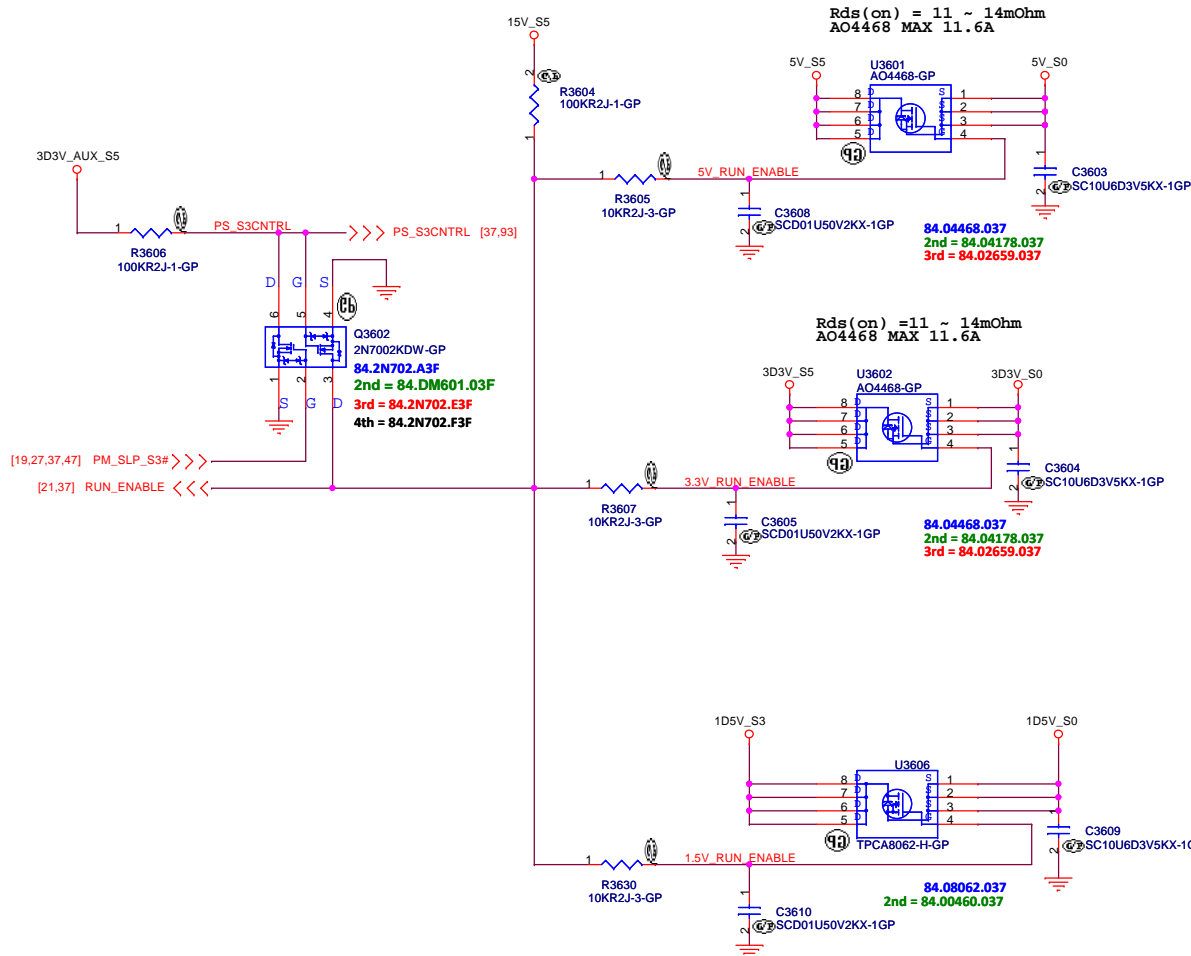
Sheet 35 of 105

**Reserved**

SSID = Reset.Suspend



## ROSA Run Power



### 5V\_S0

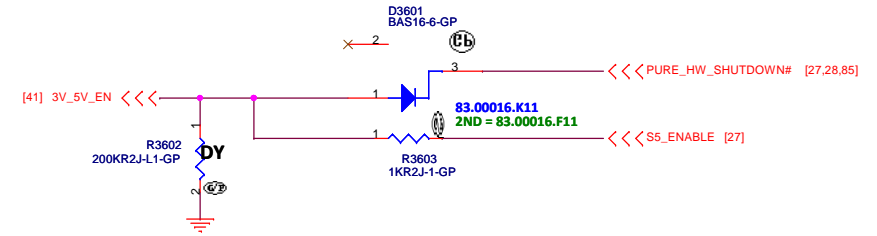
5V\_S0 Consumption  
Peak current 6A

### 3D3V\_S0

3D3V\_S0 Consumption  
Peak current 2.5A

### 1D5V\_S0

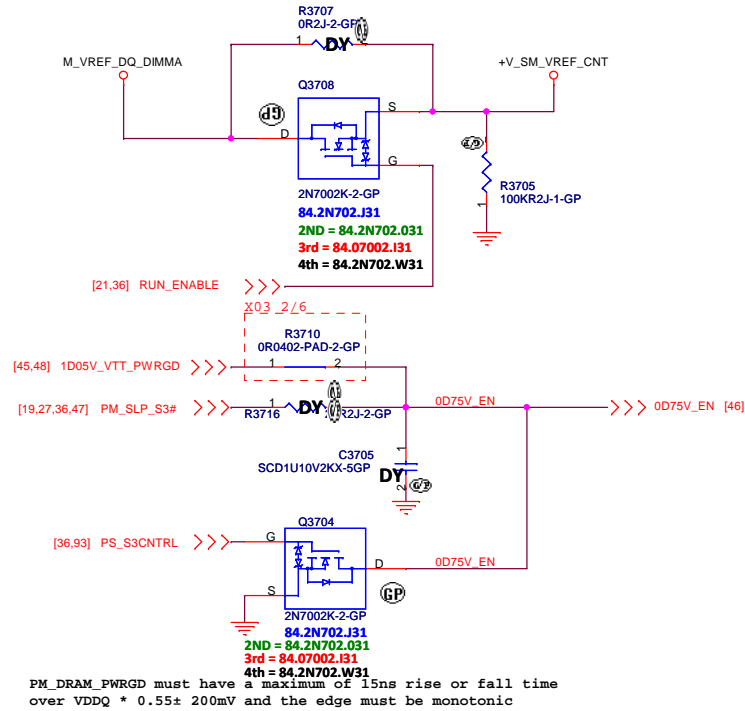
TPCA8062-H-GP MAX 28A  
Rds(on) = 4.1~5.6m Ohm  
MAX Current 6A



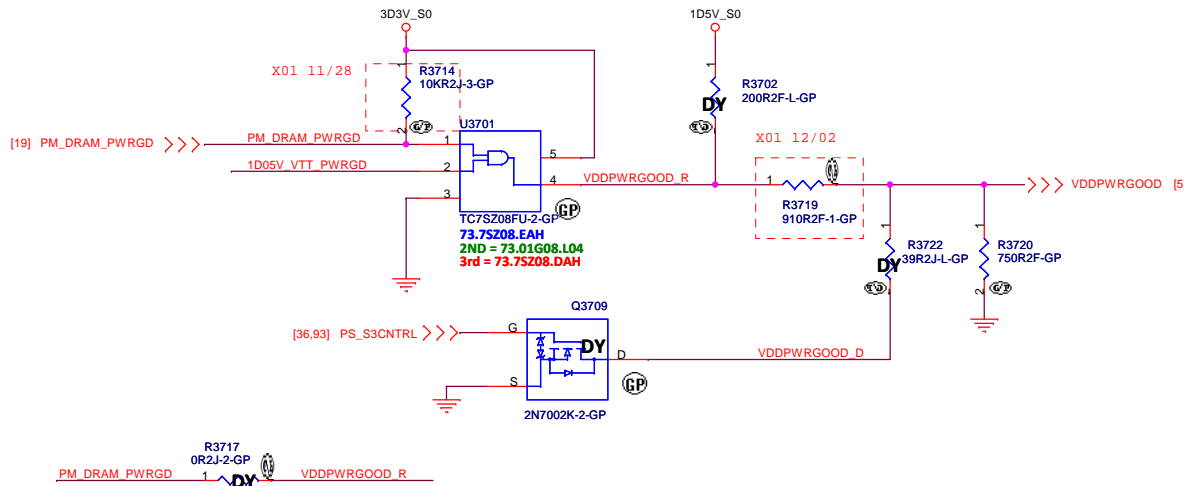
<Core Design>

SSID = Reset.Suspend

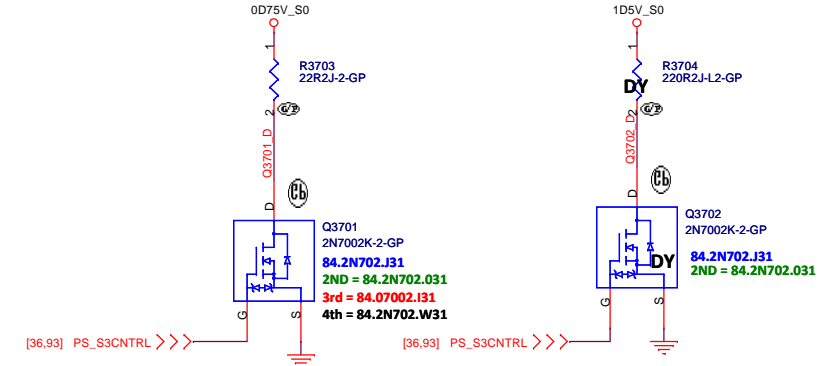
Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation



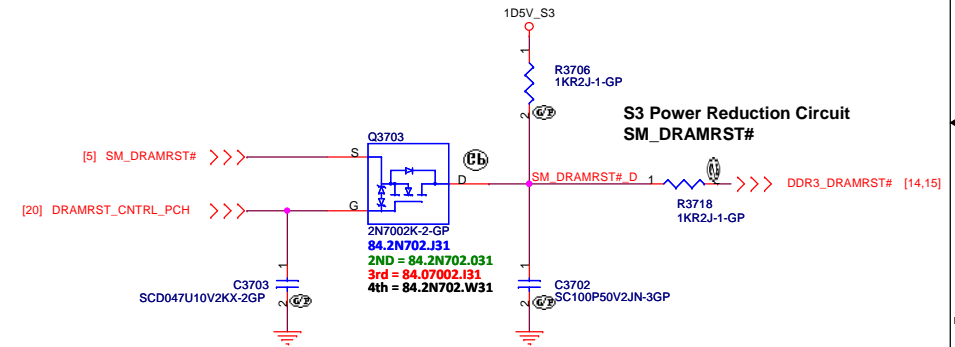
Close to CPU  
S3 Power Reduction Circuit PM\_DRAM\_PWRGD



Close to DIMM  
S3 Power Reduction Circuit PM\_DRAM\_PWRGD

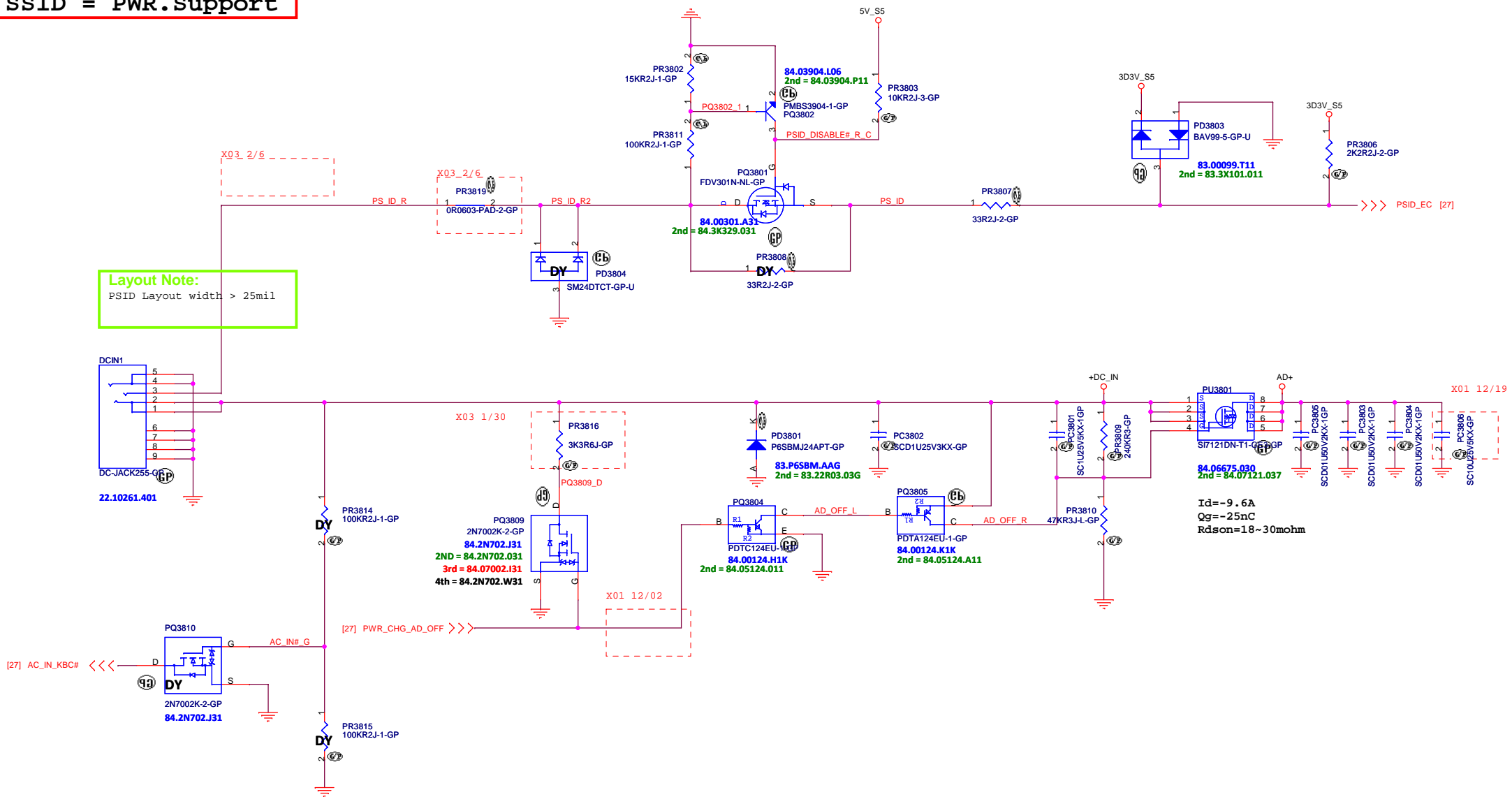


Close to CPU  
S3 Power Reduction Circuit SM\_DRAMRST#



**SSID = PWR.Support**

**Layout Note:**  
SSID Layout width > 25mil

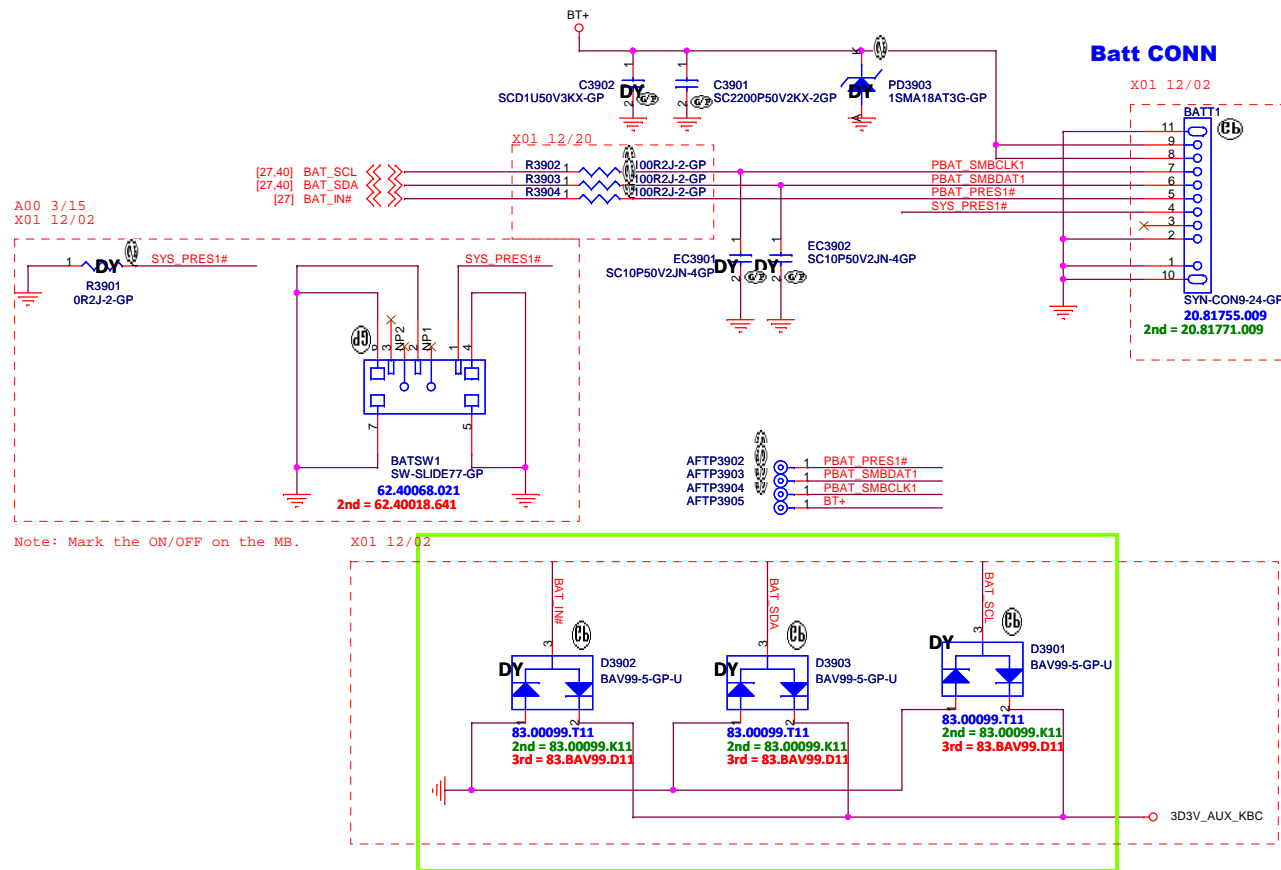


<Core Design>

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|                              |                                      |                   |
|------------------------------|--------------------------------------|-------------------|
| Title<br><b>DCIN</b>         |                                      |                   |
| Size<br>A3                   | Document Number<br><b>BMW Z4 DIS</b> | Rev<br><b>A00</b> |
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SSID = PWR.Support



Layout Note:

Place near Battery CONN

<Core Design>



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Title

**BATT CONN**

Size  
A3

Document Number

**BMW Z4 DIS**

Rev

**A00**

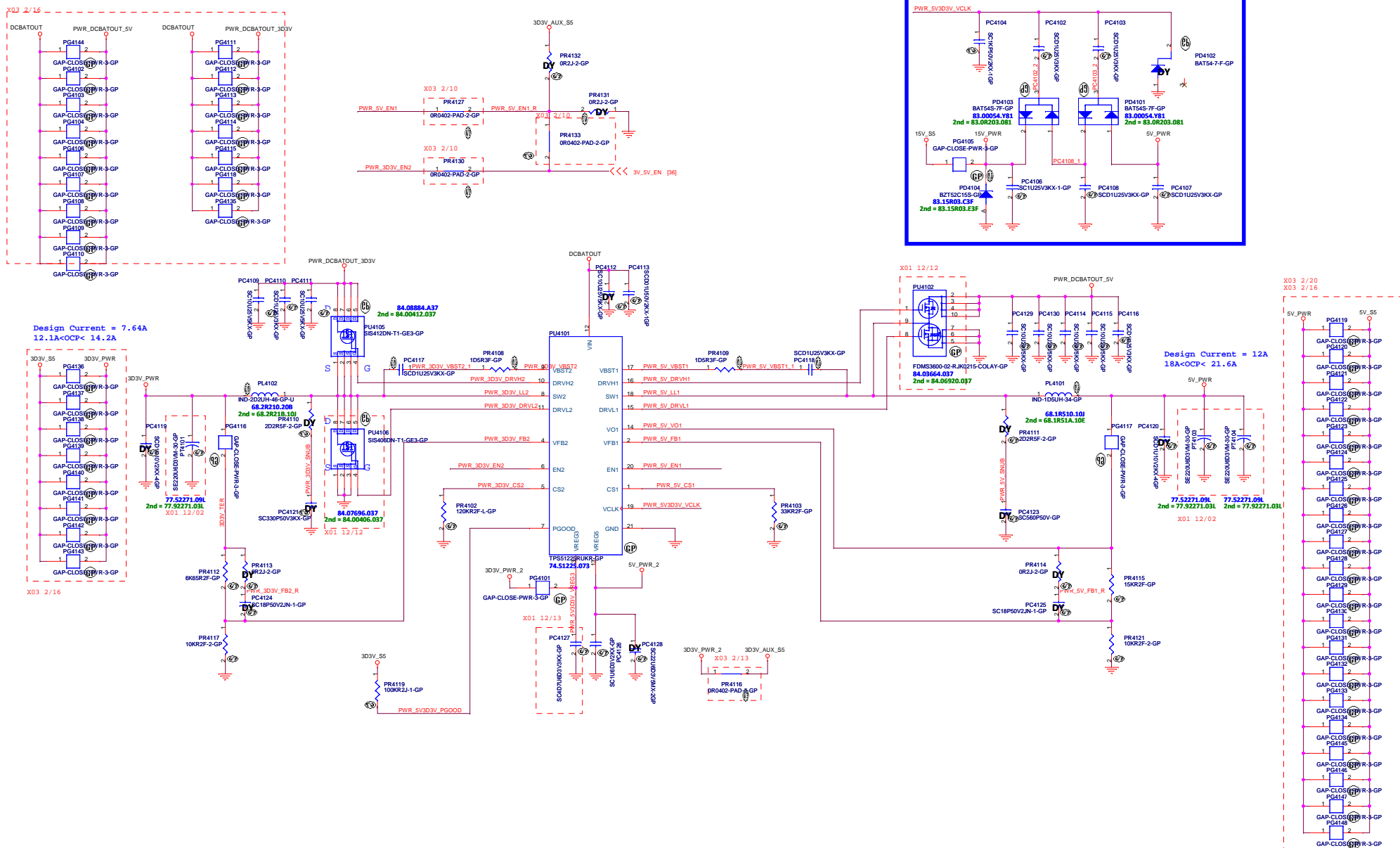
Date: Friday, March 30, 2012

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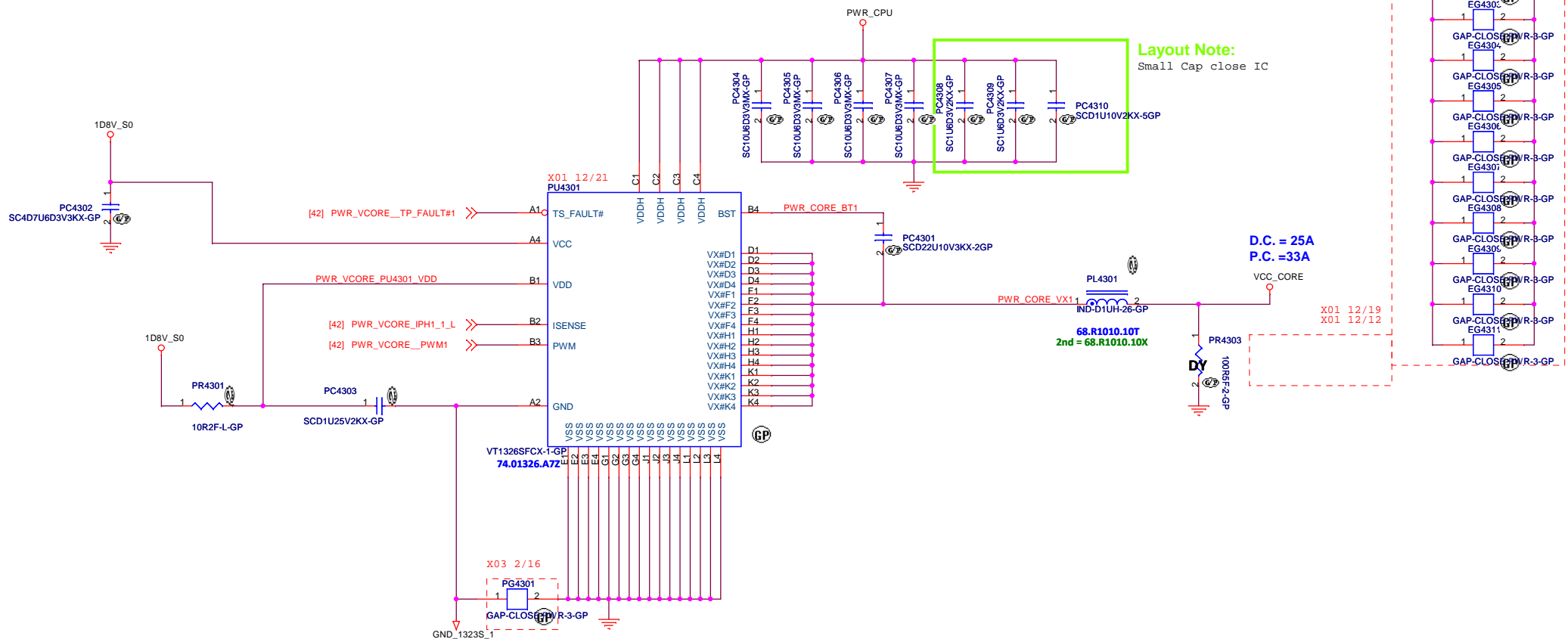


```
SSID = PWR.Plane.Regulator_5v3p3v
```





```
SSID = CPU.Regulator
```



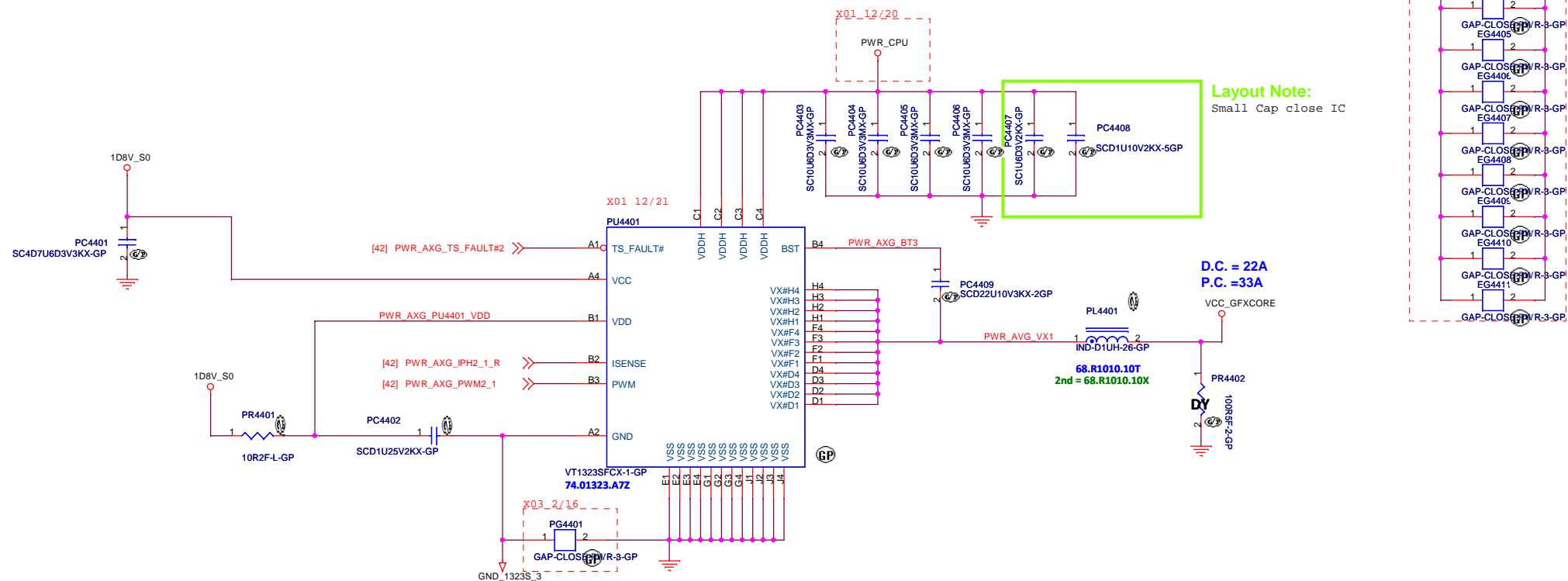
**<Core Design>**



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|       |                        |       |                              |    |     |
|-------|------------------------|-------|------------------------------|----|-----|
| Title |                        |       | VT1318+1326_CPU_CORE2+1(2/3) |    |     |
| Size  | Document Number        |       |                              |    | Rev |
| A3    | BMW Z4 DIS             |       |                              |    | A00 |
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```
SSID = CPU.Regulator
```



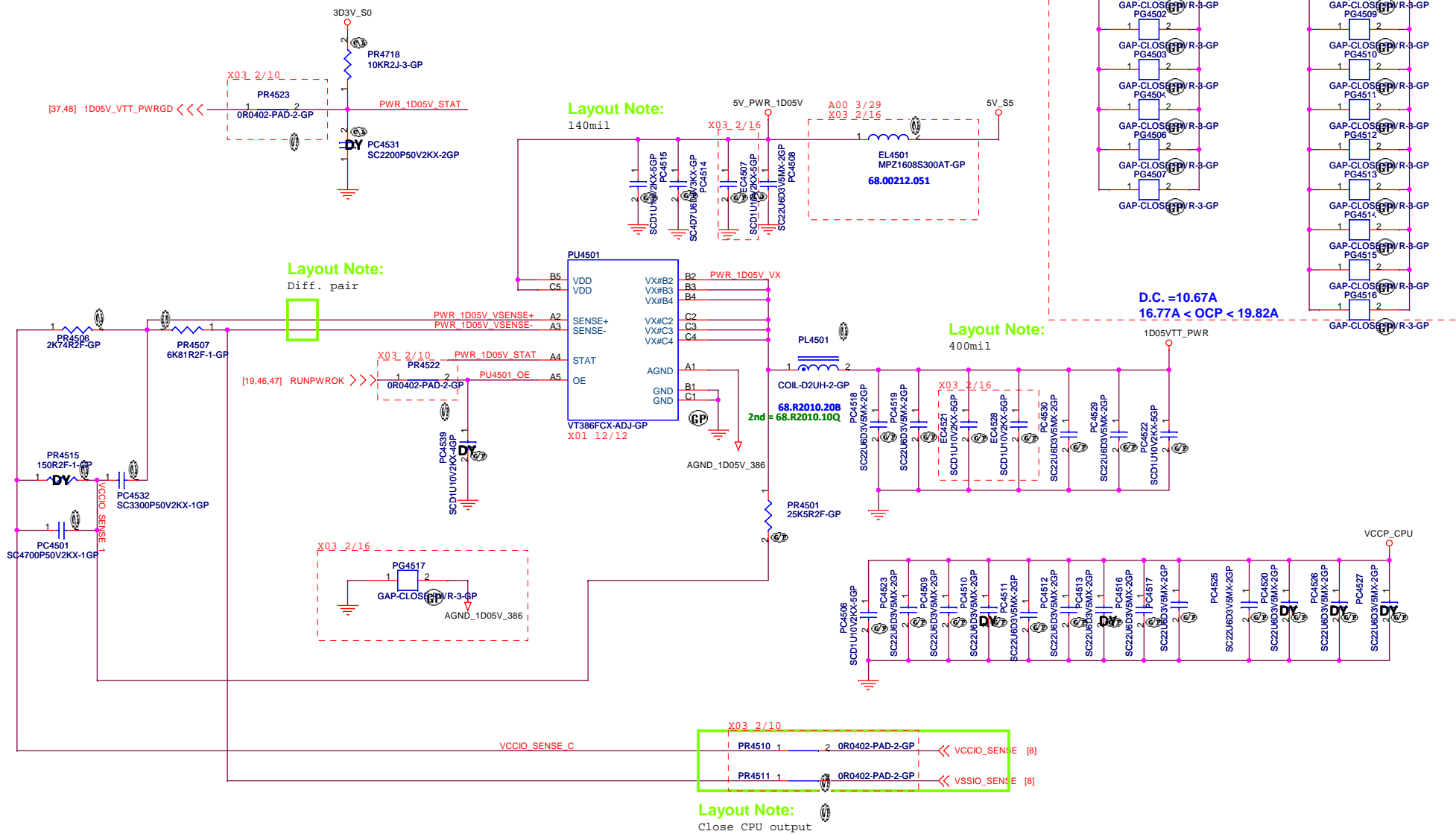
### <Core Design>



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|                              |                        |       |           |
|------------------------------|------------------------|-------|-----------|
| Title                        |                        |       |           |
| VT1318+1323_CPU_CORE1+1(3/3) |                        |       |           |
| Size                         | Document Number        | Rev   |           |
| A3                           | BMW Z4 DIS             | A     |           |
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```
SSID = PWR.Plane.Regulator_1p05v
```



<Core Design>



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Title

### 1D05V\_PCH & VCCP\_CPU

Size

| Document Number |
|-----------------|
|-----------------|

**BMW Z4 DIS**

Rev

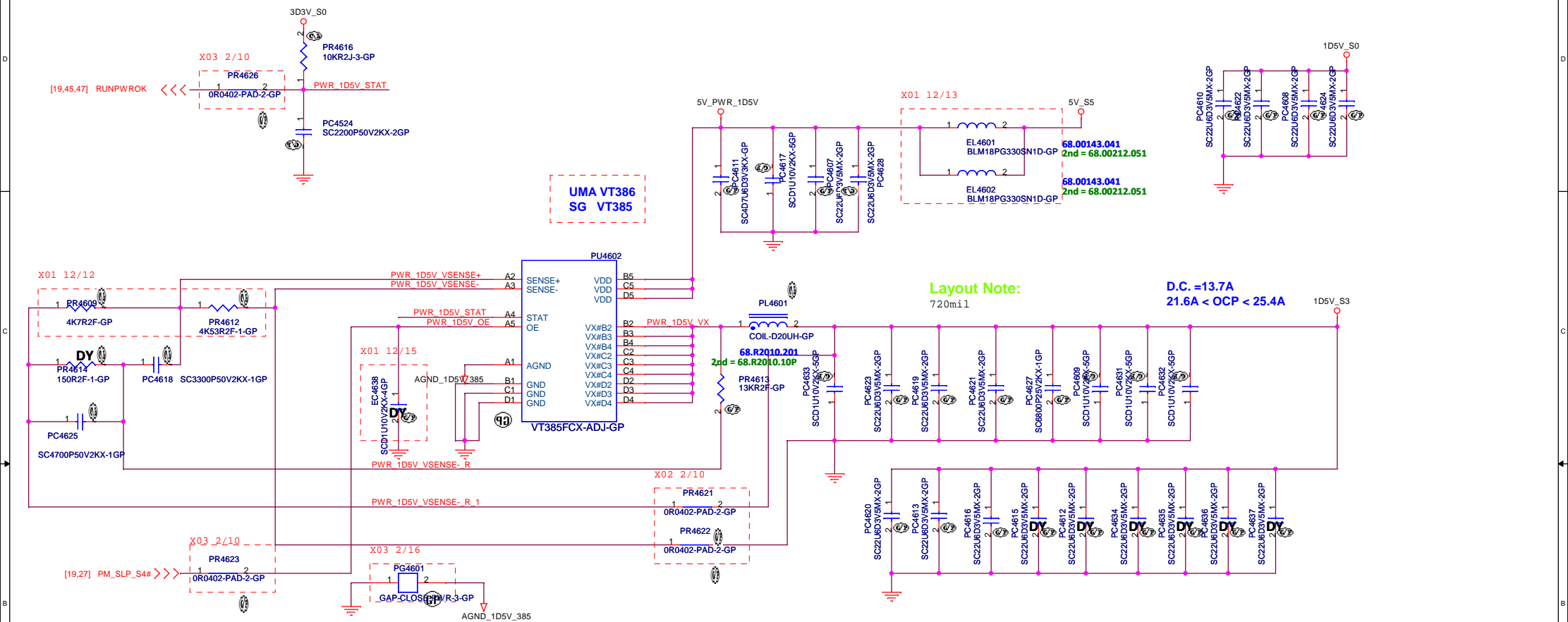
Date: Friday, March 30, 2012

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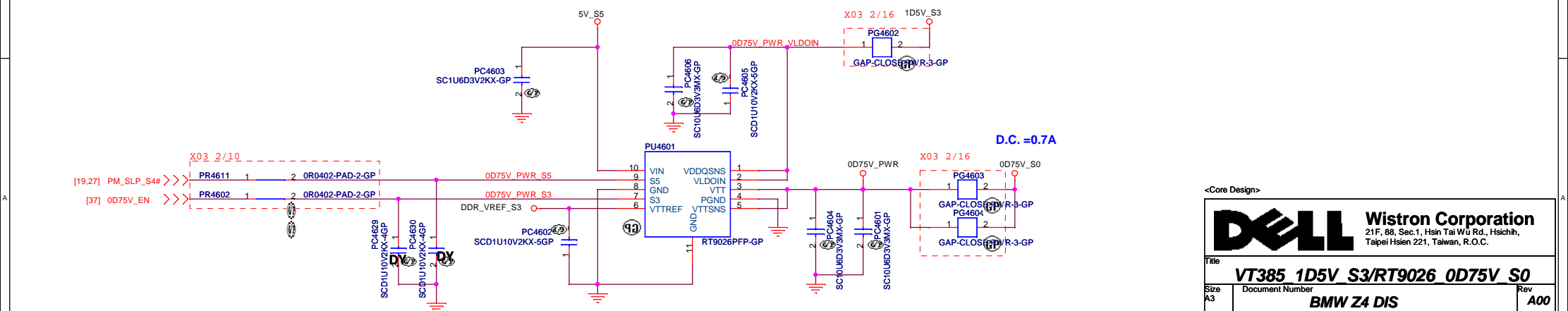
|                              |  |
|------------------------------|--|
| Date: Friday, March 30, 2012 |  |
|------------------------------|--|

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SSID = PWR.Plane.Regulator\_1p5v0p75v



## RT9026 for 0D75V\_S0



**<Core Design>**

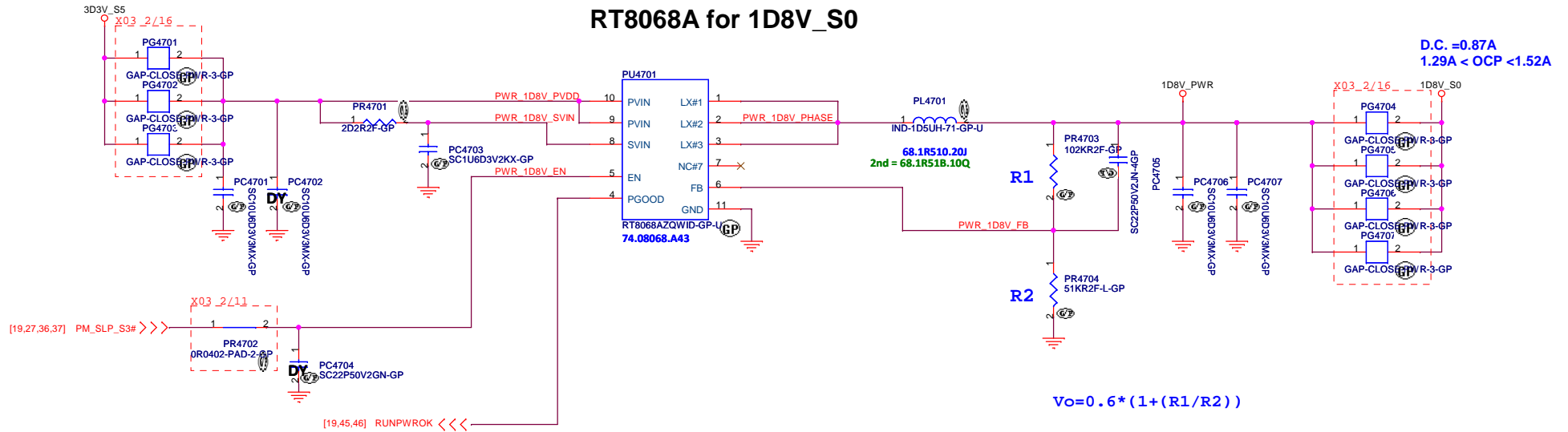


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|                                      |                        |             |     |
|--------------------------------------|------------------------|-------------|-----|
| Title                                |                        |             |     |
| <b>VT385 1D5V S3/RT9026 0D75V S0</b> |                        |             |     |
| Size<br>A3                           | Document Number        | Rev         |     |
|                                      | <b>BMW Z4 DIS</b>      | <b>A00</b>  |     |
| Date:                                | Friday, March 30, 2012 | Sheet 46 of | 105 |

SSID = PWR.Plane.Regulator\_1p8v

## RT8068A for 1D8V\_S0



<Core Design>

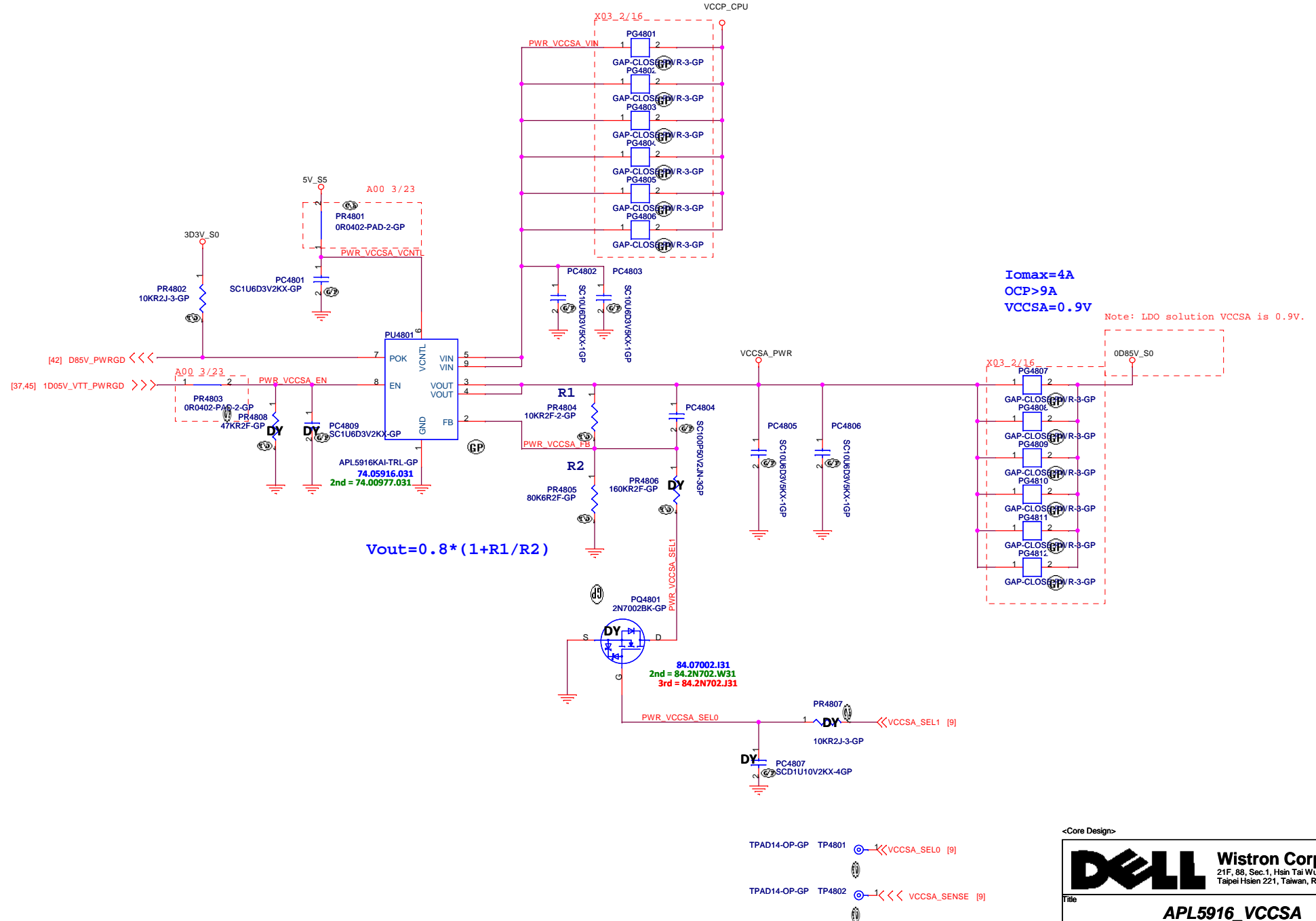


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|       |                        |       |                 |        |
|-------|------------------------|-------|-----------------|--------|
| Title |                        |       | RT8068A 1D8V_S0 |        |
| Size  | Document Number        | Rev   |                 | A00    |
| A3    | BMW Z4 DIS             |       |                 |        |
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SSID = PWR.Plane.Regulator\_vccsa

X02 1/9



<Core Design>



|       |                        |            |                      |        |
|-------|------------------------|------------|----------------------|--------|
| Title |                        |            | <b>APL5916 VCCSA</b> |        |
| Size  | Document Number        | Rev        |                      |        |
| A3    | <b>BMW Z4 DIS</b>      | <b>A00</b> |                      |        |
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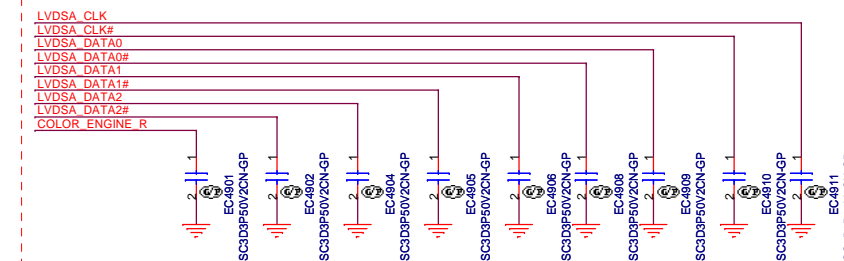


**SSID = VIDEO**



**Layout Note:**  
Trace width = 80mil

## Camera Power



**<Core Design>**



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|   |       |
|---|-------|
| 1 | Title |
|---|-------|

### **LCD Connector**

Size

|  |                 |
|--|-----------------|
|  | Document Number |
|--|-----------------|

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Title

**CRT Connector**

Size  
A3

Document Number  
**BMW Z4 DIS**

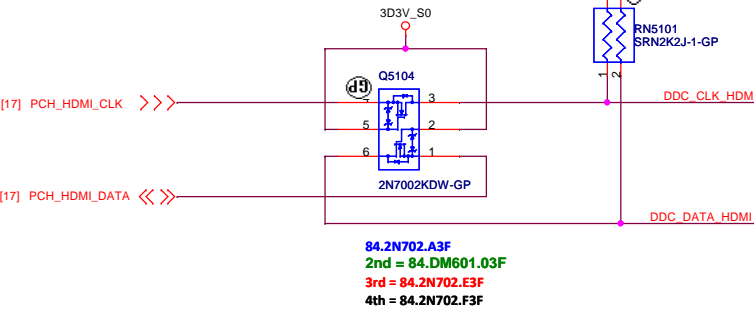
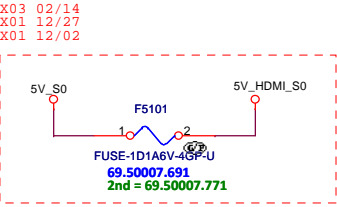
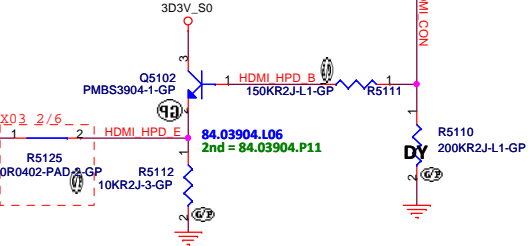
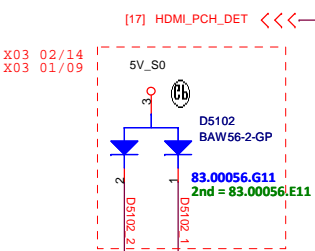
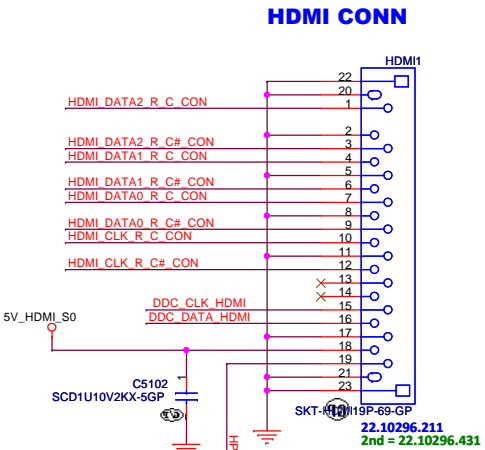
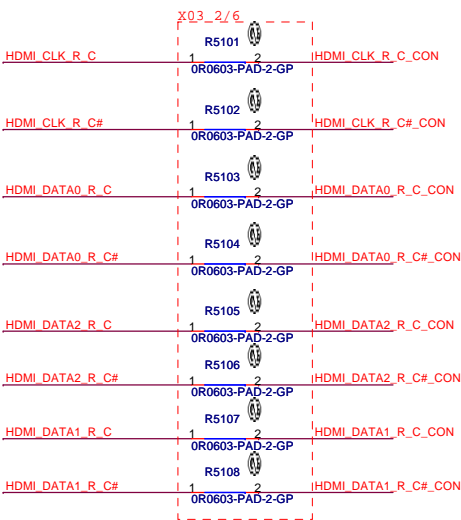
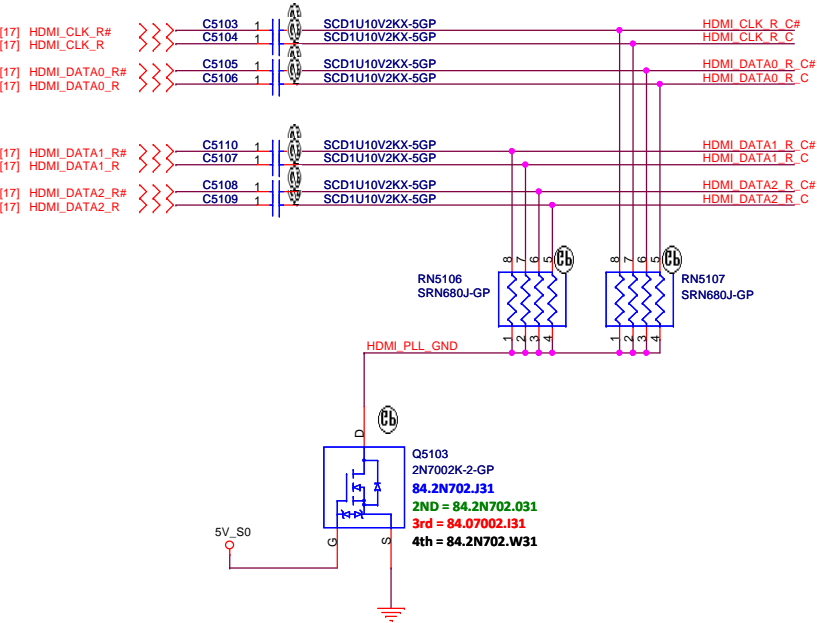
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# SSID = VIDEO

## HDMI Level Shifter



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**BMW Z4 DIS**

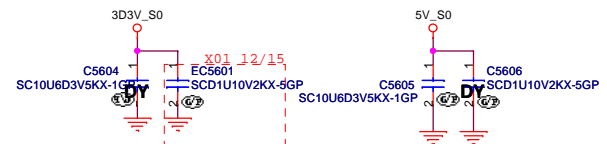
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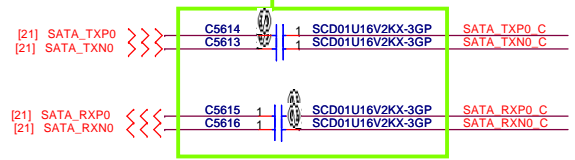
**ITP/Fan Connector**

SSID = SATA

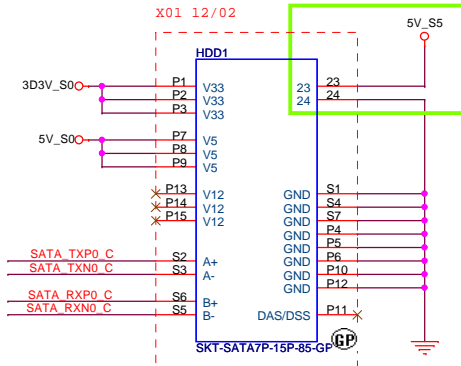


Layout Note:

AC coupling Cap:  
place near CONN(<100mils)



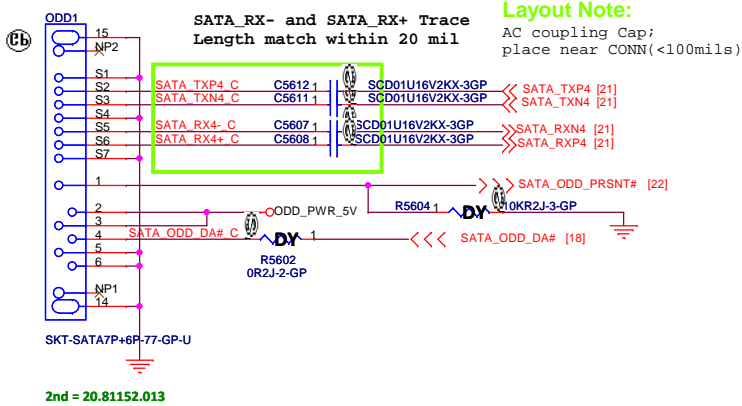
HDD CONN



Due to layout, HDD1 pin 23 modify 5V\_S5

20.81599.022  
2nd = 22.10300.C51

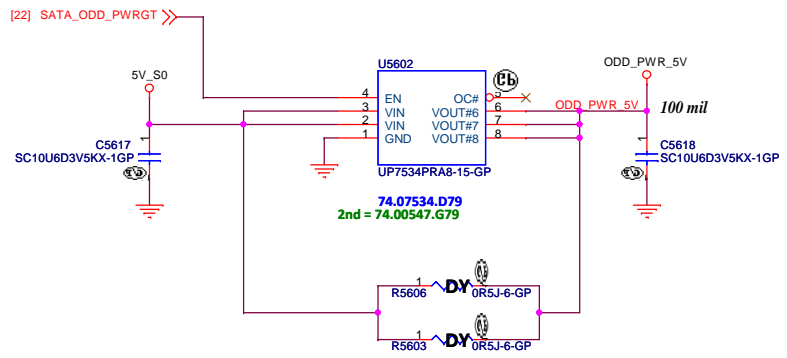
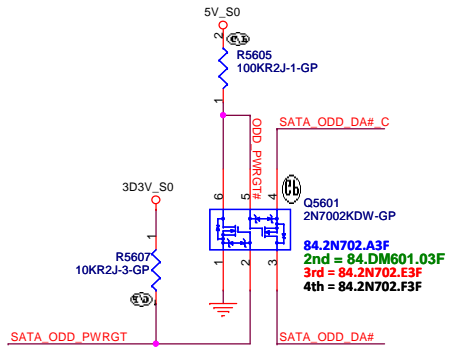
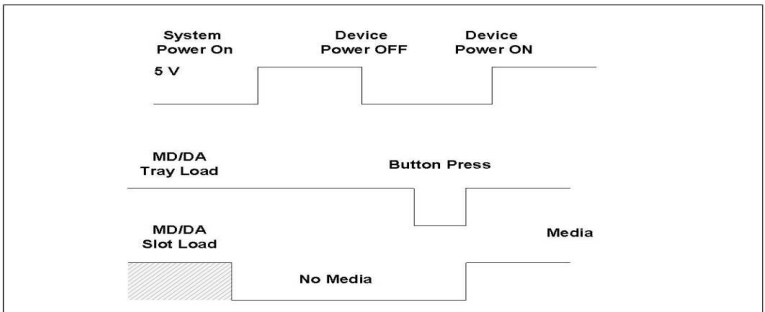
ODD CONN



Layout Note:

AC coupling Cap:  
place near CONN(<100mils)

Zero Power ODD Power Sequence



<Core Design>

|                                 |                                      |   |                   |
|---------------------------------|--------------------------------------|---|-------------------|
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| Title<br><b>HDD/ODD</b>         |                                      |   |                   |
| Size<br>A3                      | Document Number<br><b>BMW Z4 DIS</b> |   | Rev<br><b>A00</b> |
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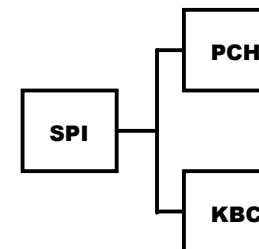
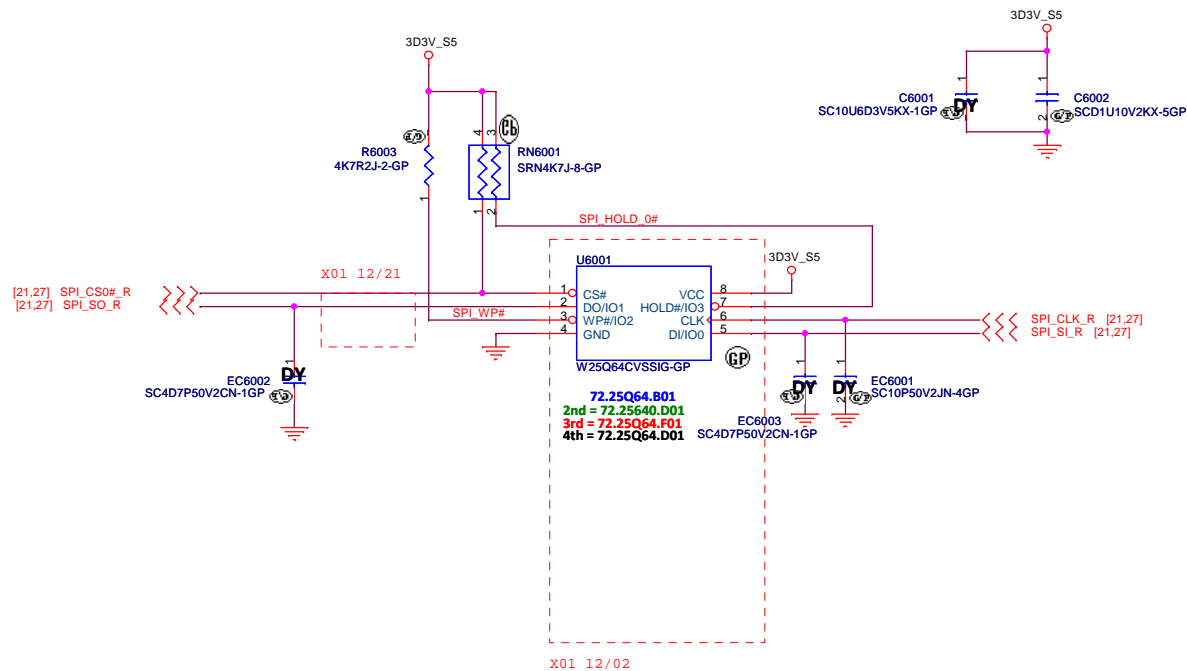
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**Reserved**



SSID = Flash.ROM

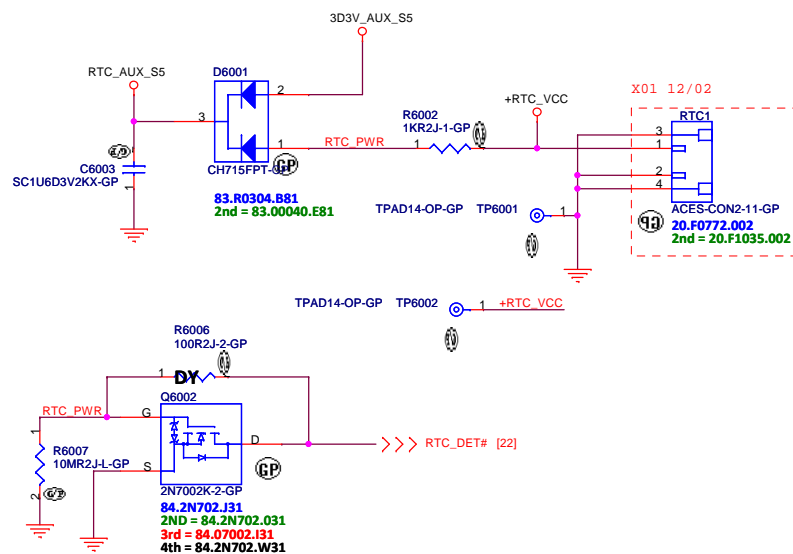
### SPI Flash ROM(8M) for PCH



#### Layout Note:

KBC---10"---PCH  
KBC---1.5"~6.5"---SPI  
PCH---0.5"~6.5"---SPI

SSID = RBATT



<Core Design>



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**Flash/RTC**

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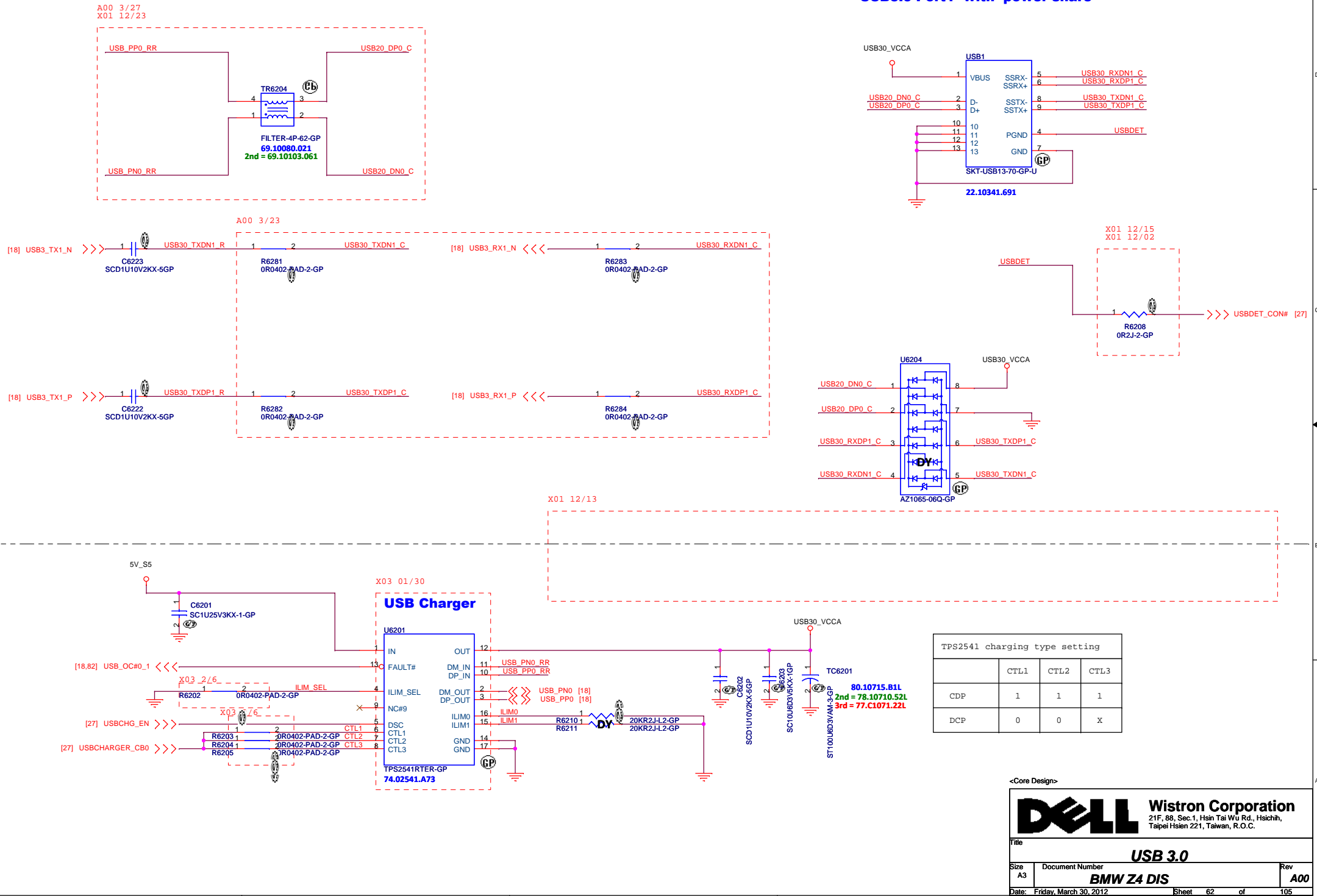
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SSID = USB

## USB3.0 Port1 with power share



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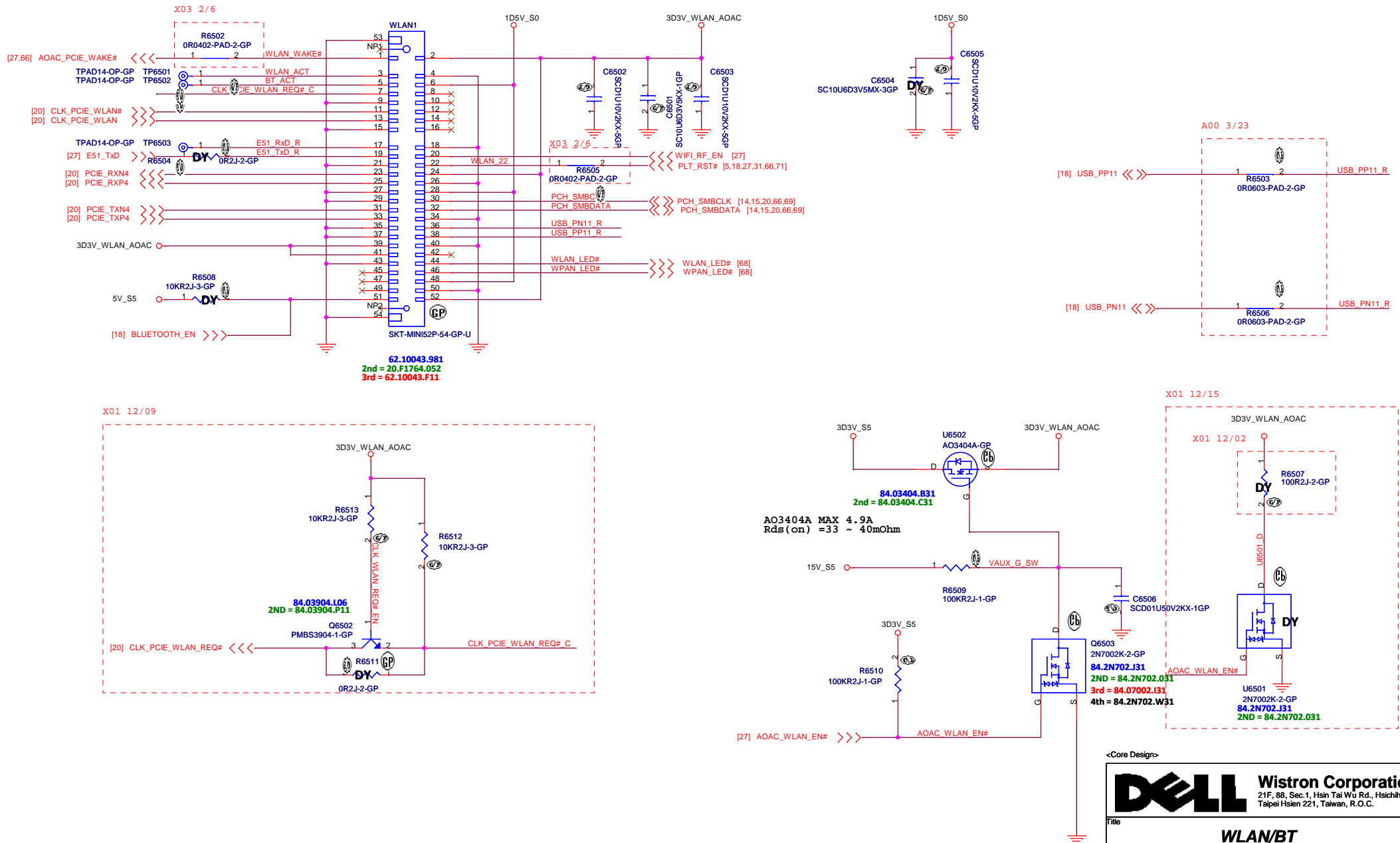
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SSID = Wireless

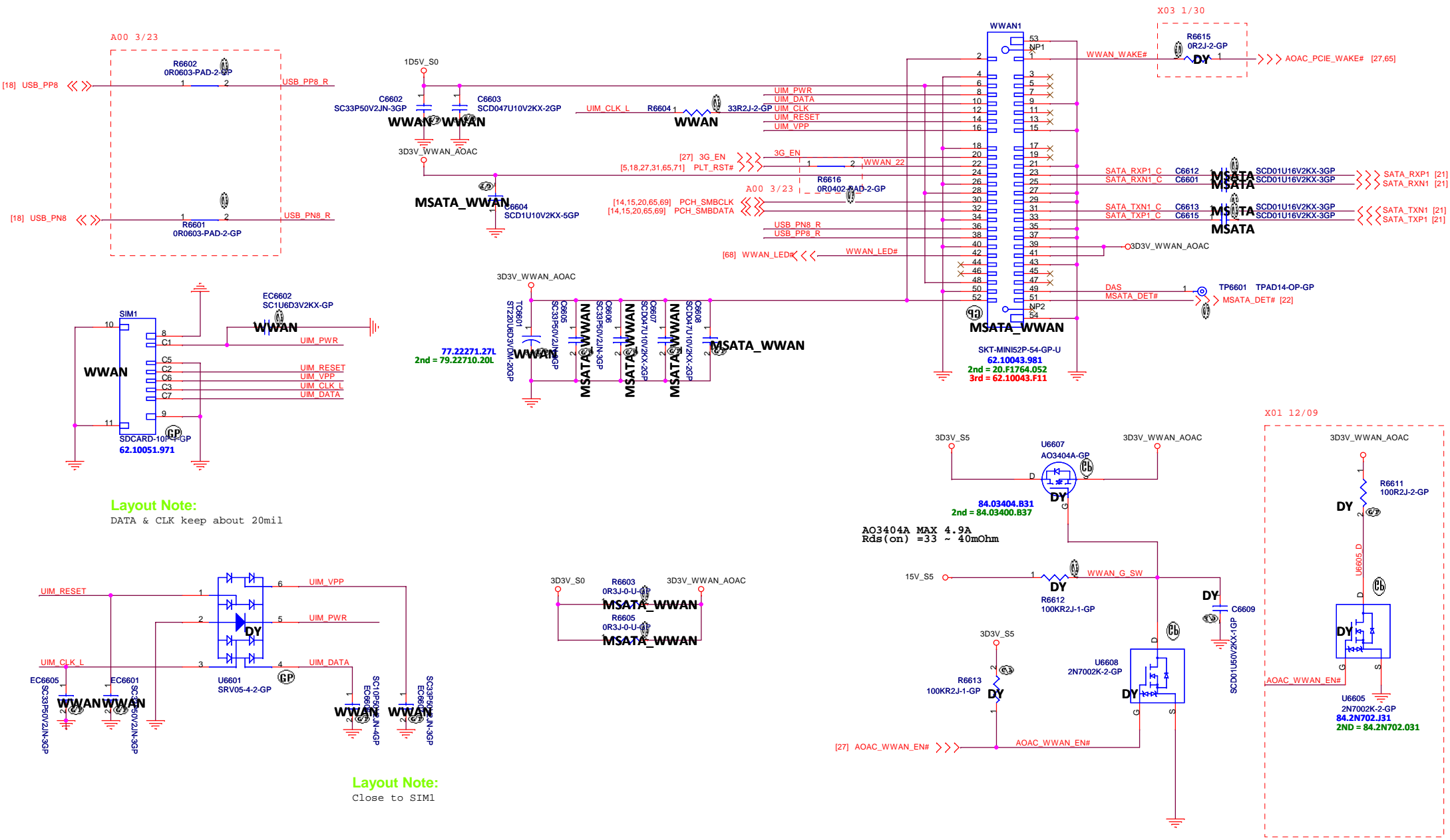
# Mini Card Connector(802.11a/b/g/n)

## WLAN CONN



<Core Design>

# SSID = Wireless



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Title

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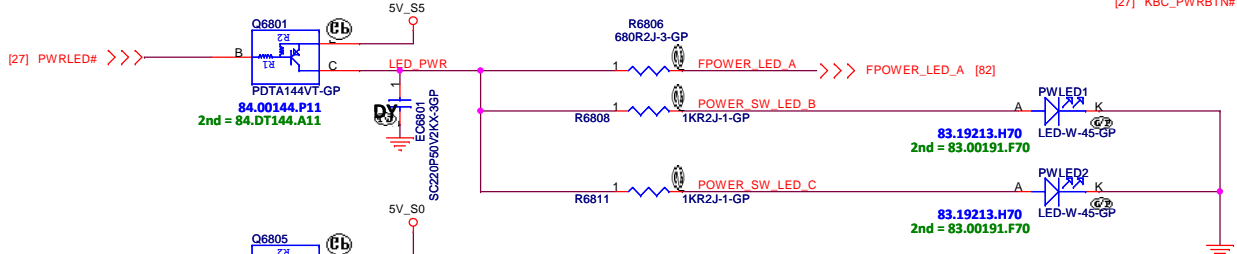
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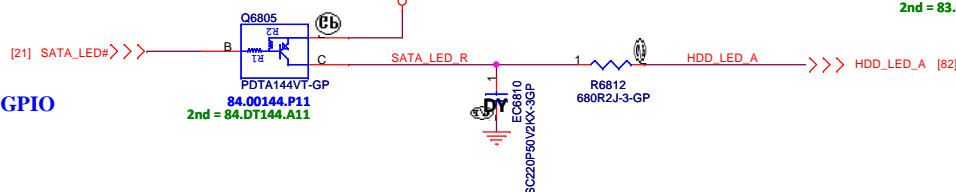
**Reserved**

SSID = User.Interface

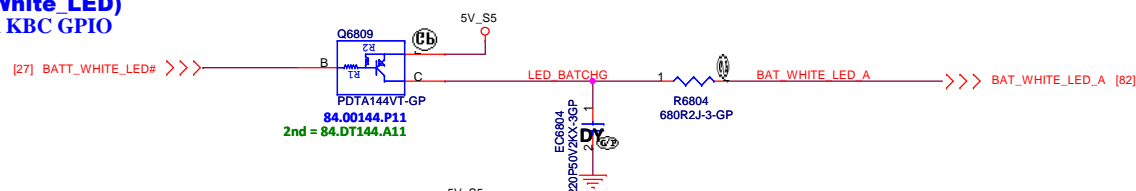
Front Power LED  
LOW acted from KBC GPIO



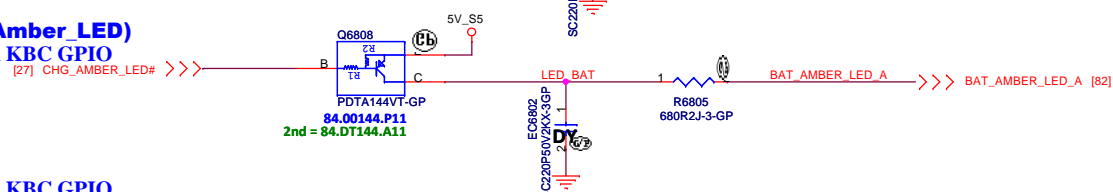
SATA HDD LED  
LOW acted from PCH GPIO



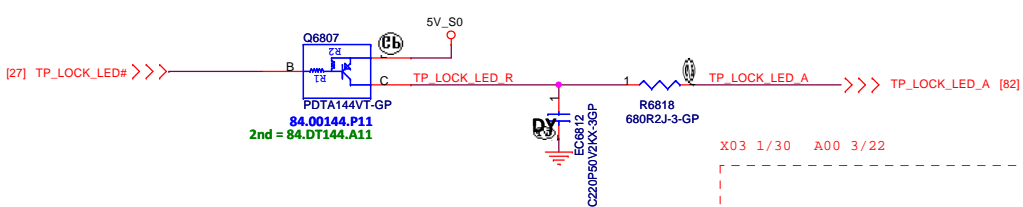
Battery LED2(White\_LED)  
LOW acted from KBC GPIO



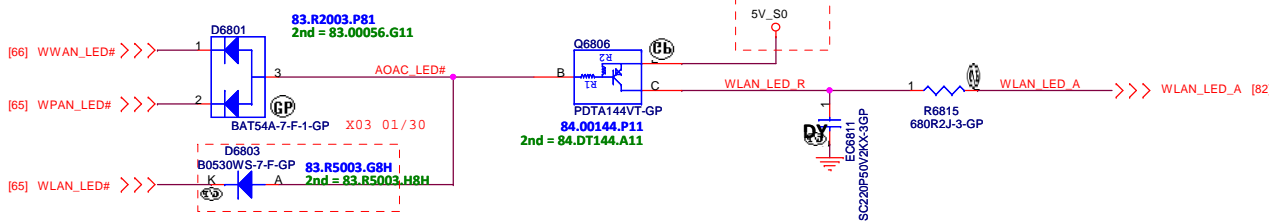
Battery LED1(Amber\_LED)  
LOW acted from KBC GPIO



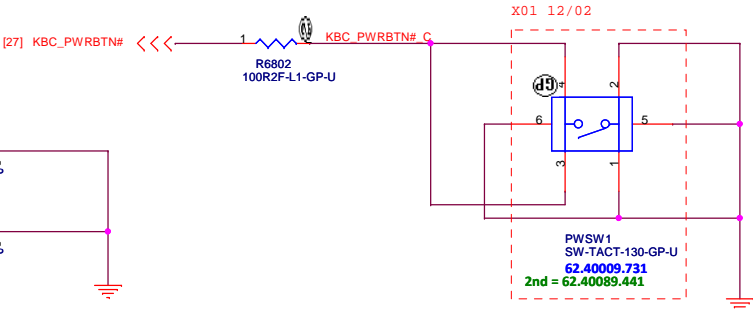
TPLOCK LED  
LOW acted from KBC GPIO



WLAN LED  
LOW acted from KBC GPIO

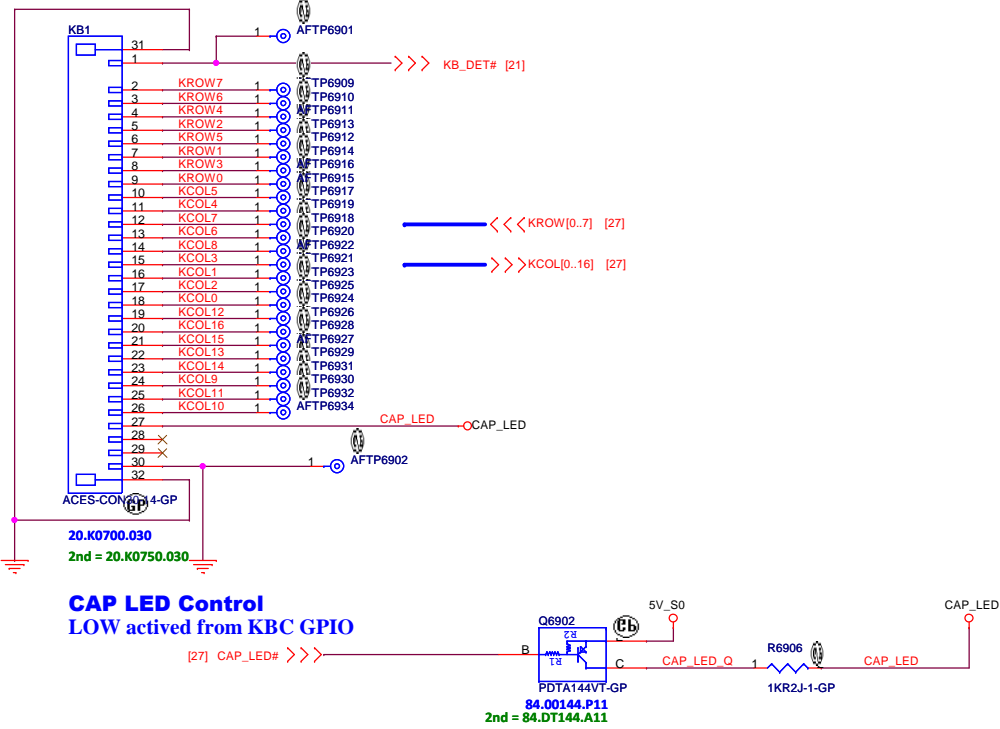


PWRBTN



SSID = KBC

### Internal Keyboard Connector

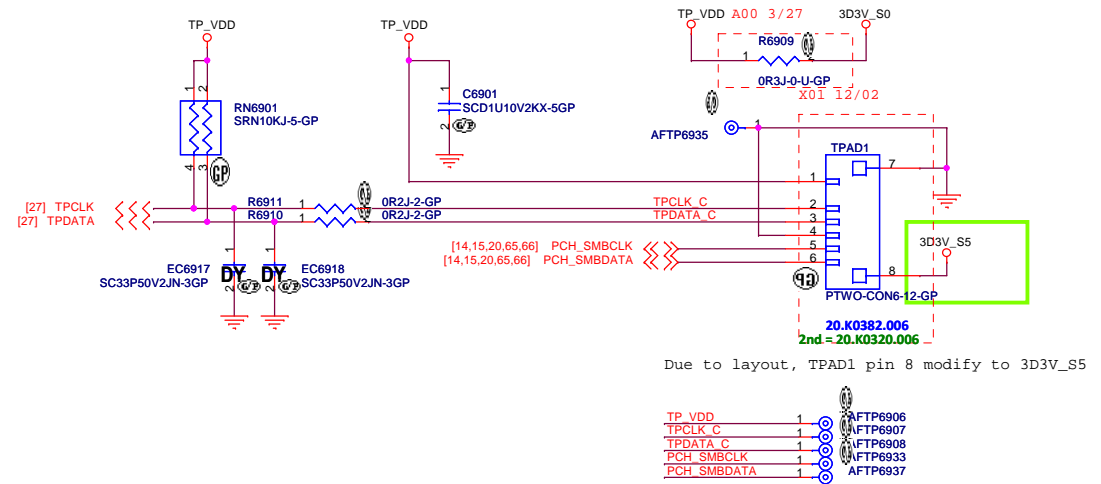


### CAP LED Control

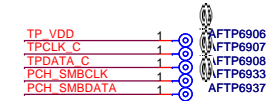
LOW acted from KBC GPIO

SSID = Touch.Pad

### Touch Pad Connector

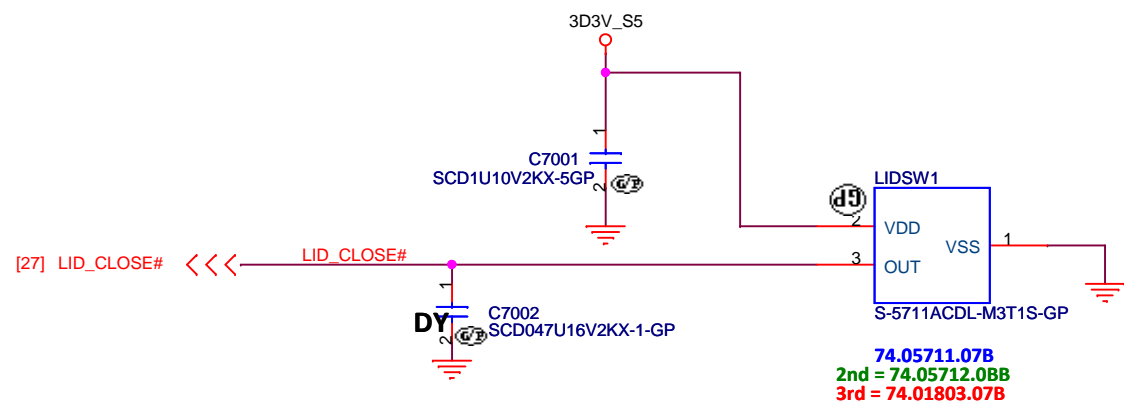


Due to layout, TPAD1 pin 8 modify to 3D3V\_S5




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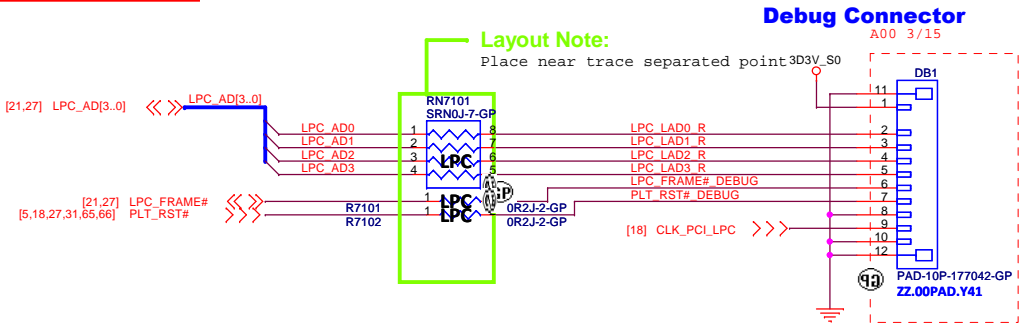
SSID = User.Interface



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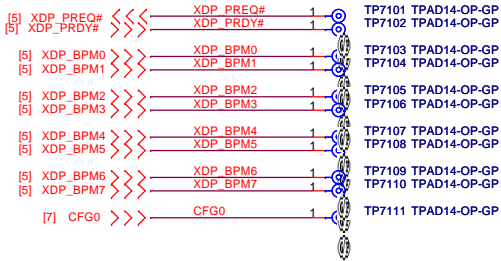
|   |                                      |   |                   |
|---|--------------------------------------|---|-------------------|
|  |                                      | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title<br><b>Hall Sensor</b>   |                                      |   |                   |
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SSID = DEBUG PORT



SSID = CPU

**CPU XDP**



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Title

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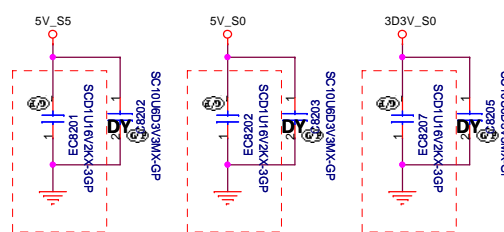
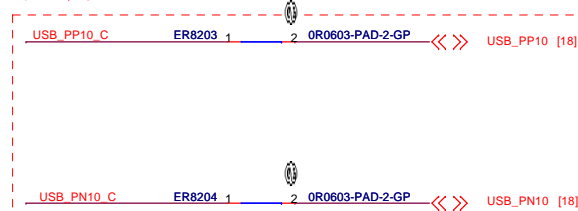
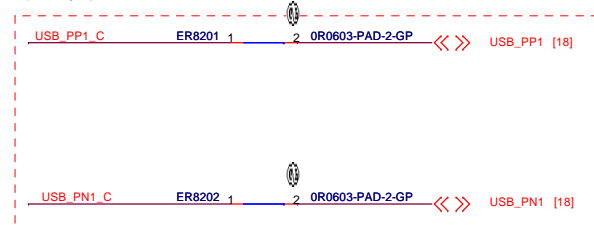
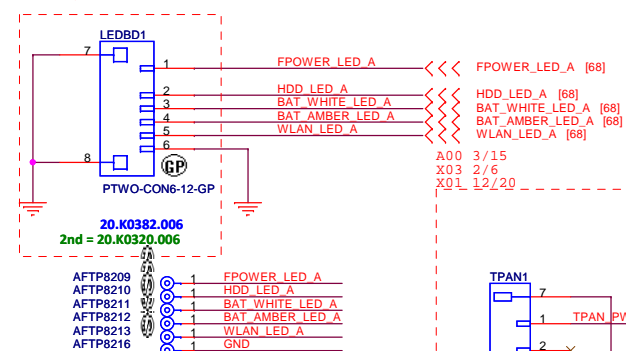
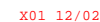
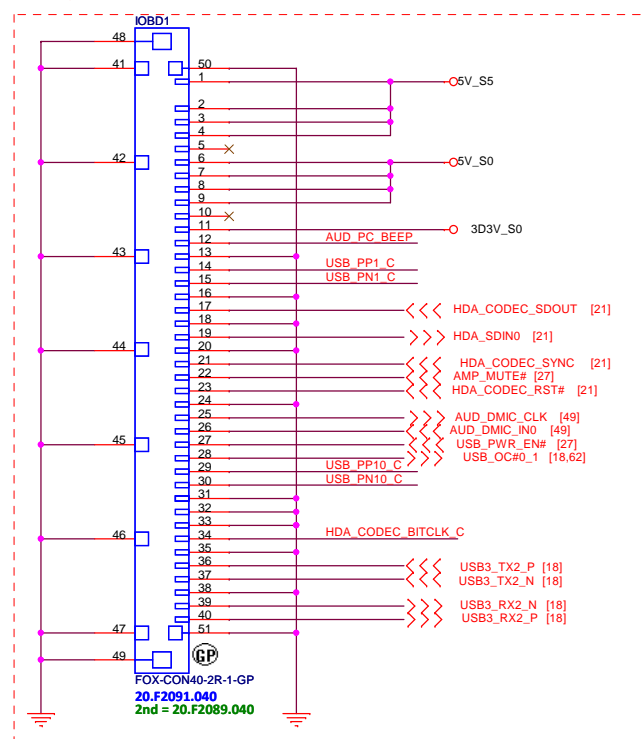
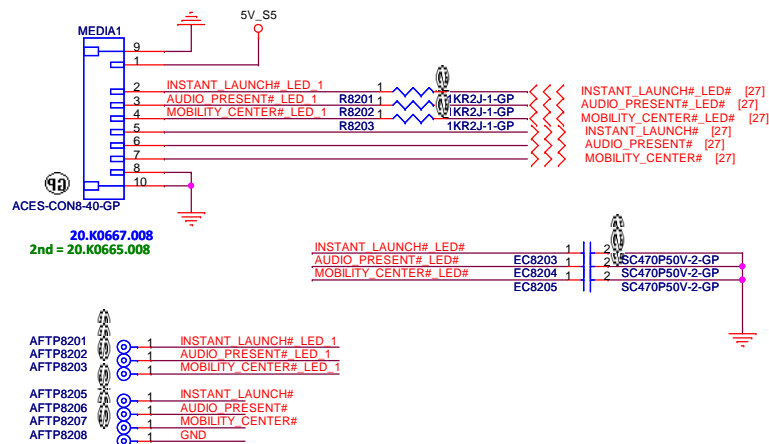
Rev  
**A00**

Date: Friday, March 30, 2012

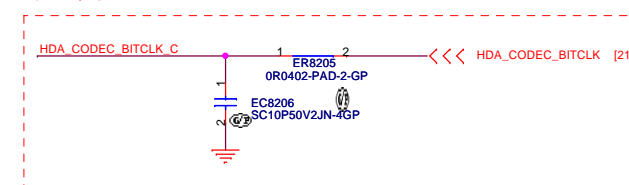
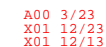
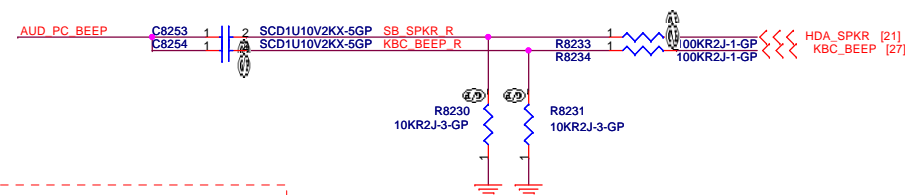
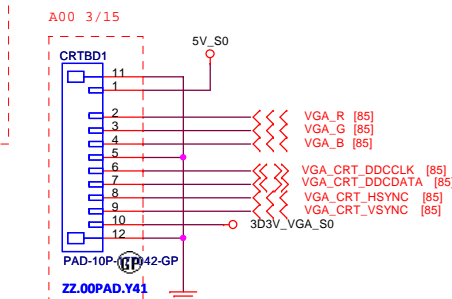
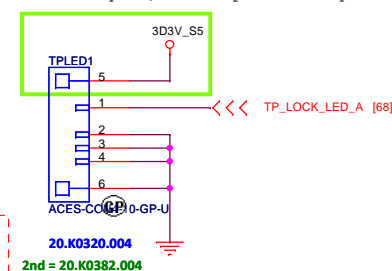
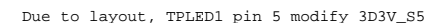
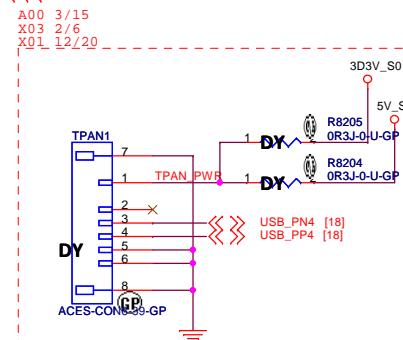
Sheet 81 of 105

**Reserved**

```
SSID = User.Interface
```



X01 12/09 Request by EMI



**<Core Design>**



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Title

Size  
ADocument Number **BMV**

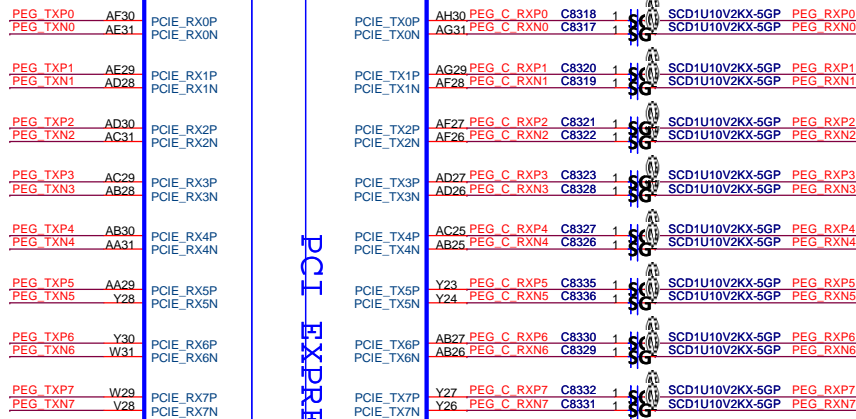
Date: Friday, March 30, 2012

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|     |      |
|-----|------|
| Rev | 1.00 |
|-----|------|

SSID = VIDEO

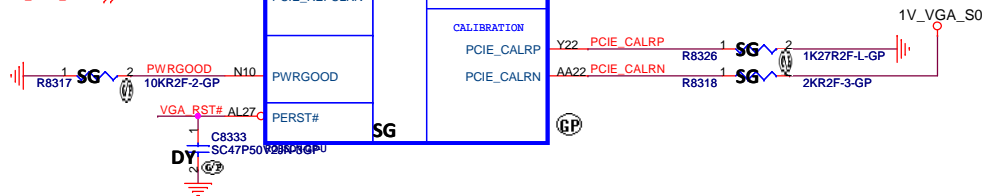
[4] PEG\_TXP[7..0] >> >> PEG\_RXP[7..0] [4]  
[4] PEG\_TXN[7..0] >> >> PEG\_RXN[7..0] [4]



PCI EXPRESS INTERFACE

X01 12/15

[22] DGPU\_HOLD\_RST# >> >> X03\_2/6 >> 0R0402-PAD-2-GP >> VGA\_RST# [85]



<Core Design>

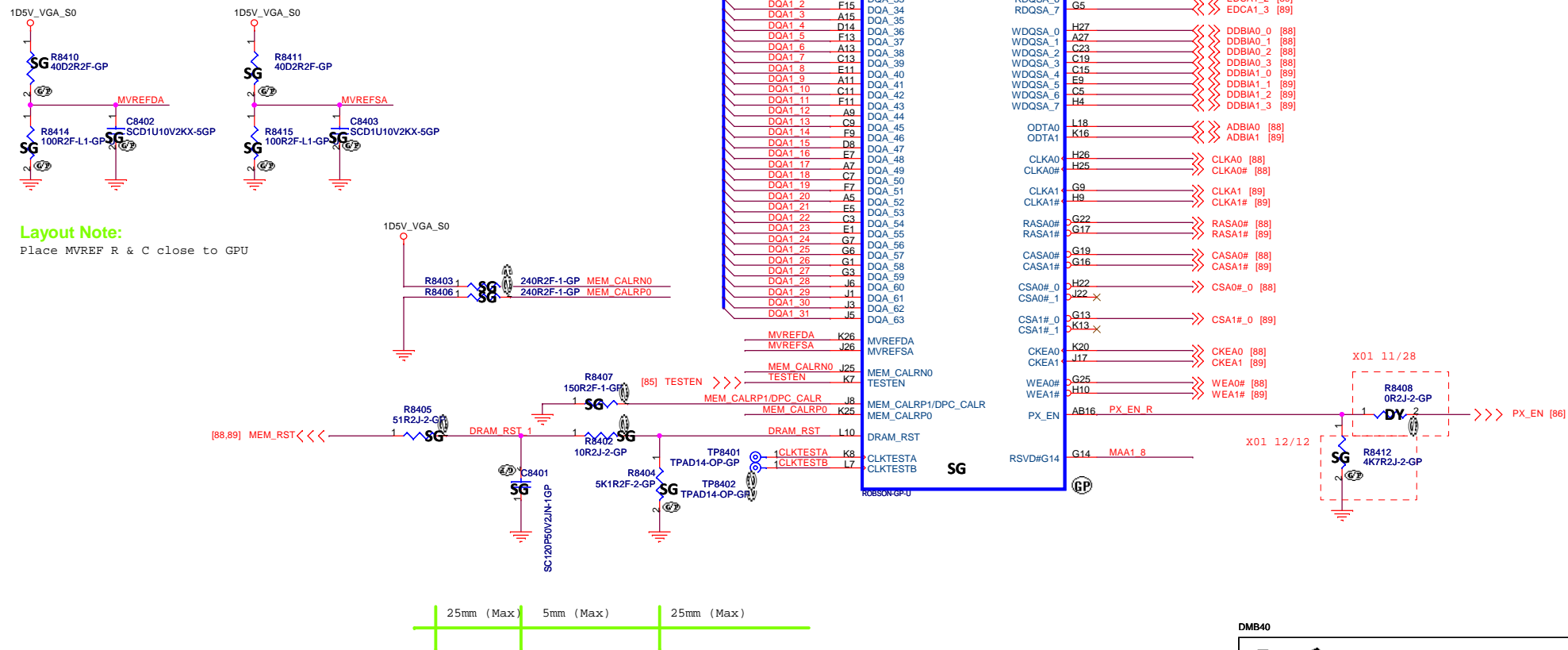
**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU PEG/STRAPPING(1/5)**

Size: A3 Document Number: **BMW Z4 DIS** Rev: **A00**

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**SSID = VIDEO**



**Layout Note:**

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R\_MEM\_2



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Title

## GPU Memory(2/5)

Size  
A

|                 |  |
|-----------------|--|
| Document Number |  |
|-----------------|--|

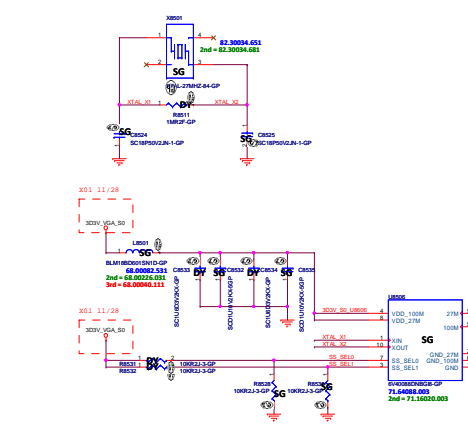
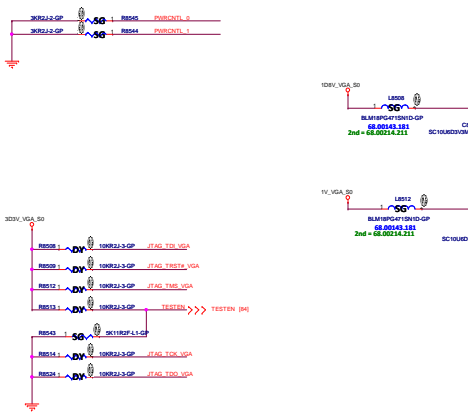
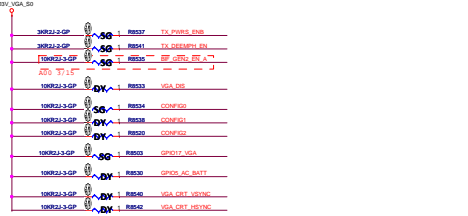
## BMW Z4 DIS

Date: Friday, March 30, 2012

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| CONFIGURATION STRAPS  |               |  |             |                  |
|---|---------------|--|-------------|------------------|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET |               |  |             |                  |
| STRAPS  | PIN           | DESCRIPTION OF DEFAULT SETTINGS  | RECOMMENDED | PLATFORM RESET   |
| TX_PWRS_ENB   | GPIO0         | Transmitter Power Savings Enable<br>0: 50% Tx output swing 1: Full Tx output swing   | X           | 1                |
| TX_DEEMPH_EN  | GPIO1         | PCIe TRANSMITTER DE-EMPHASIS ENABLED<br>0: Tx de-emphasis disabled 1: Tx de-emphasis enabled   | X           | 1                |
| BIF_GEN2_EN_A   | GPIO2         | 0: Advertises the PCIe device as 2.50G/s capable at power on<br>1: Advertises the PCIe device as 5.00G/s capable at power on           | 0           | 0                |
| GPIO5_AC_BATT   | GPIO5         | optional input allow the system to request a fast power reduction by setting GPIO5 to low  | ?           | 0                |
| GPIO8_ROMSO   | GPIO8         | 0: VGA Controller capacity enabled<br>1: The device won't be recognized as the system's VGA controller                                 | 0           | 0                |
| VGA_DIS   | GPIO9         | 0: Disable external BIOS ROM device<br>1: Enable external BIOS ROM device  | X           | 0                |
| ROMIDCFG2_0   | GPIO[13:11]   | BIOS ROM ID Config[2] defines the ROM type<br>ROM_ROM_0, ROM_ROM_1, ROM_ROM_2 defines the primary memory aperture size                 | X X X       | 0 0 1<br>(250MB) |
| GPIO21_BB_EN  | GPIO21        | RESERVED   | 0           | 0                |
| BIOS_ROM_EN   | GPIO22_ROMCEN | 0: Disable external BIOS ROM device<br>1: Enable external BIOS ROM device  | X           | 0                |
| VP_DEVICE_STRAP_IN  | VZSYNC        | VP Device Strap Enable Indicate to the software driver that it sense whether or not a VP device is connected on the VP Host interface. | X           | 0                |
| RSVD  | H2SYNC        | RESERVED   | 0           | 0                |
| RSVD  | GENERICC      | RESERVED   | 0           | 0                |
| AUD[1]  | HSYNC         | AUD[1:0]:11-Audio for both DisplayPort and HDMI  | X           | 1                |
| AUD[0]  | VSYNC         |  | X           | 1                |

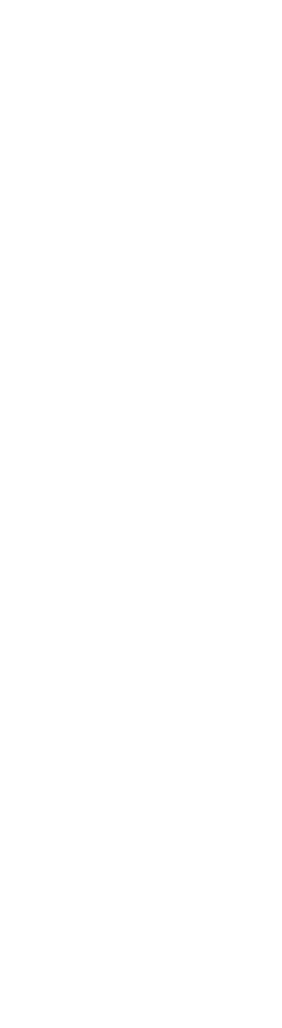
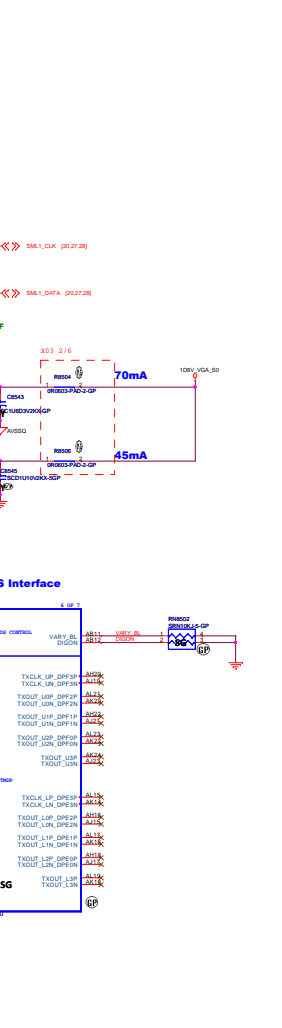
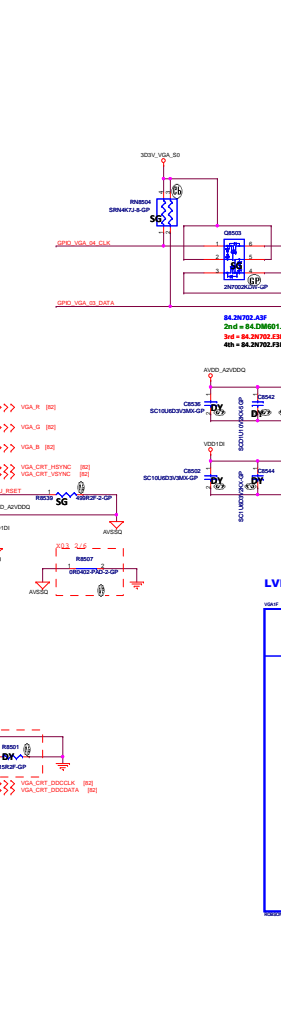
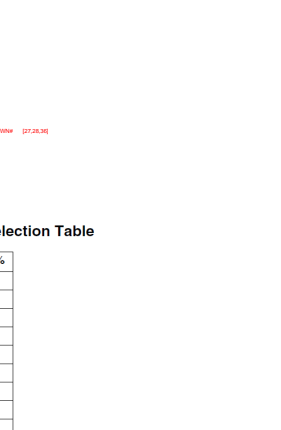
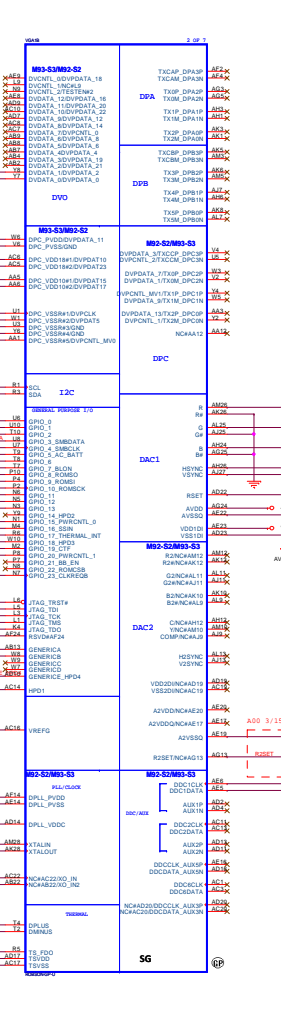
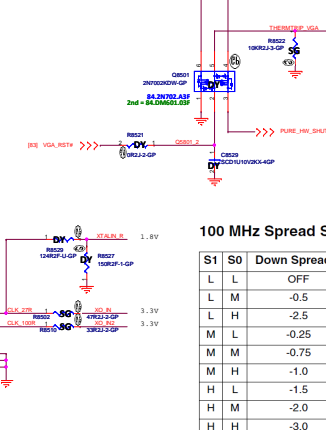
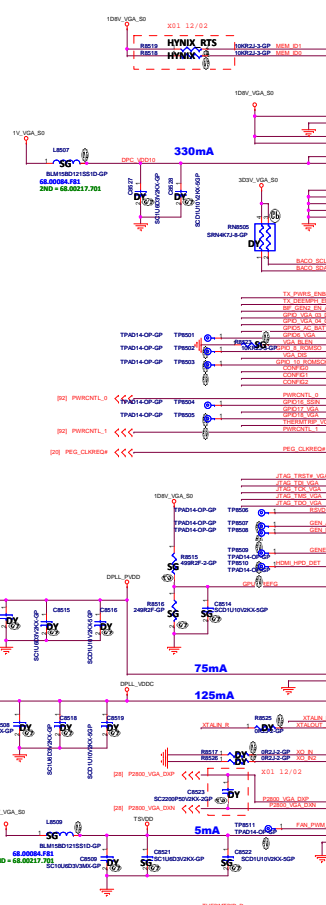
Straps Pin



MEMORY ID Table

| DVPPDATA[3:0] | Description                                    |
|---------------|--|
| 0011          | GD0R5 1.250GHz RynLx-H5Q2H24MFR-T2C 128M*16    |
| 0001          | GD0R5 1.250GHz RynLx-H5Q2H24MFR-T2C 128M*16    |
| 0000          | GD0R5 1.250GHz SAM000N-R4G20325FD-PC04 128M*16 |

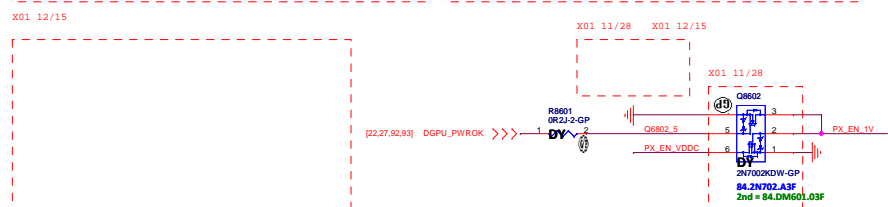
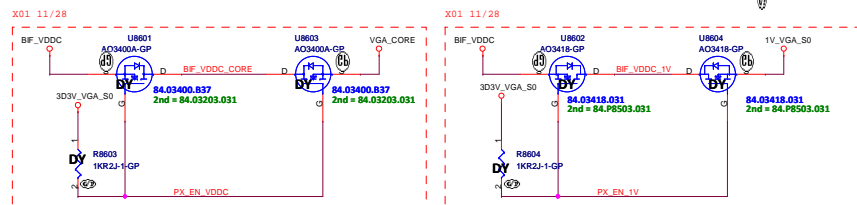
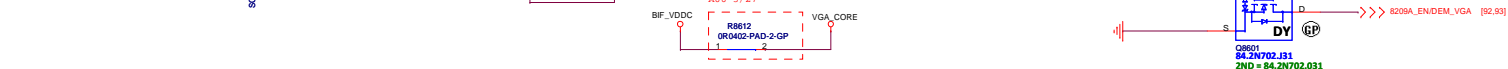
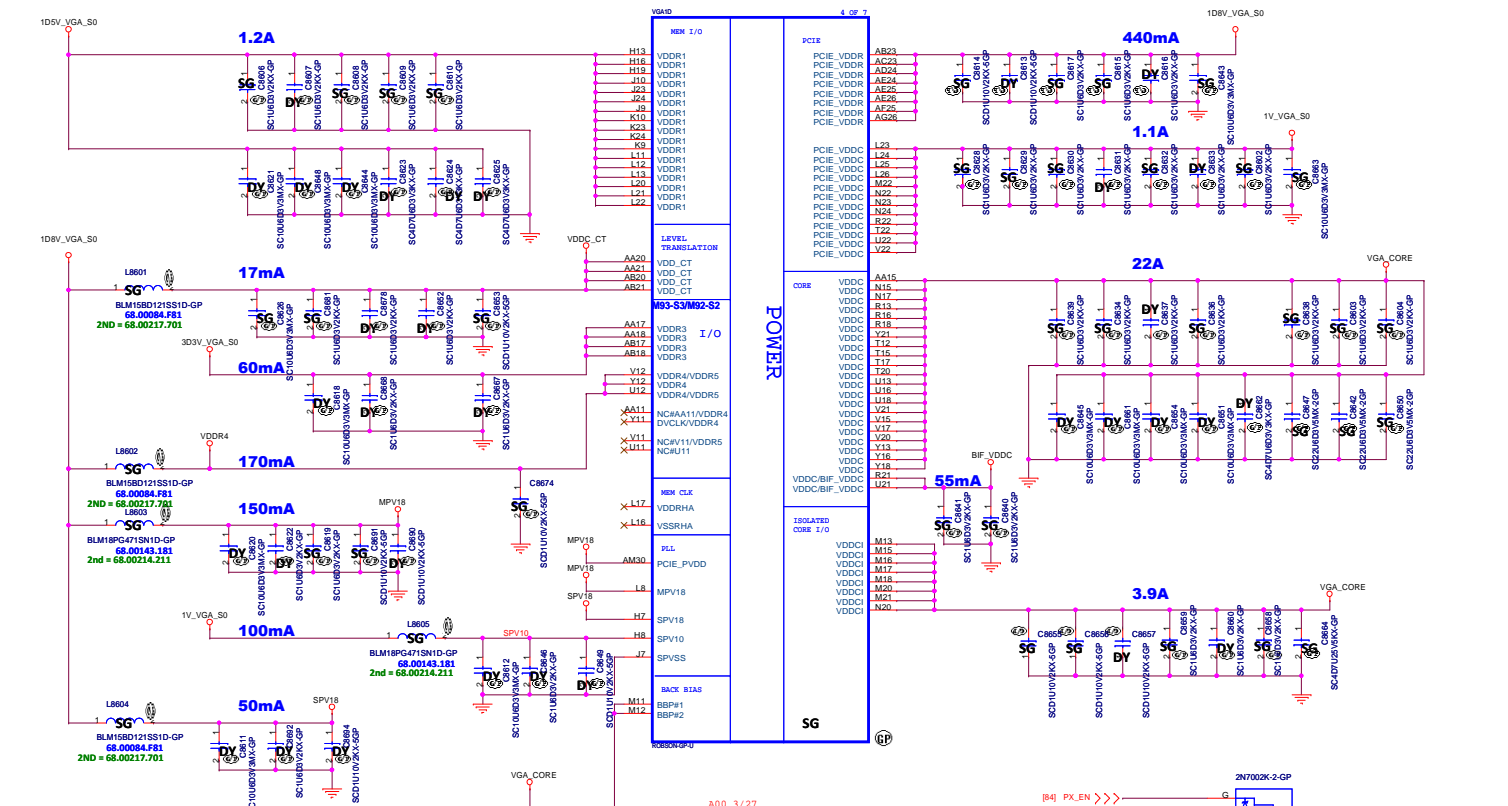
DVPPDATA[0:3] Default: Pull down



100 MHz Spread Selection Table

| S1 | S0 | Down Spread% |
|----|----|--------------|
| L  | L  | OFF          |
| L  | M  | -0.5         |
| L  | H  | -2.5         |
| M  | L  | -0.25        |
| M  | M  | -0.75        |
| M  | H  | -1.0         |
| H  | L  | -1.5         |
| H  | M  | -2.0         |
| H  | H  | -3.0         |

## SSID = VIDEO



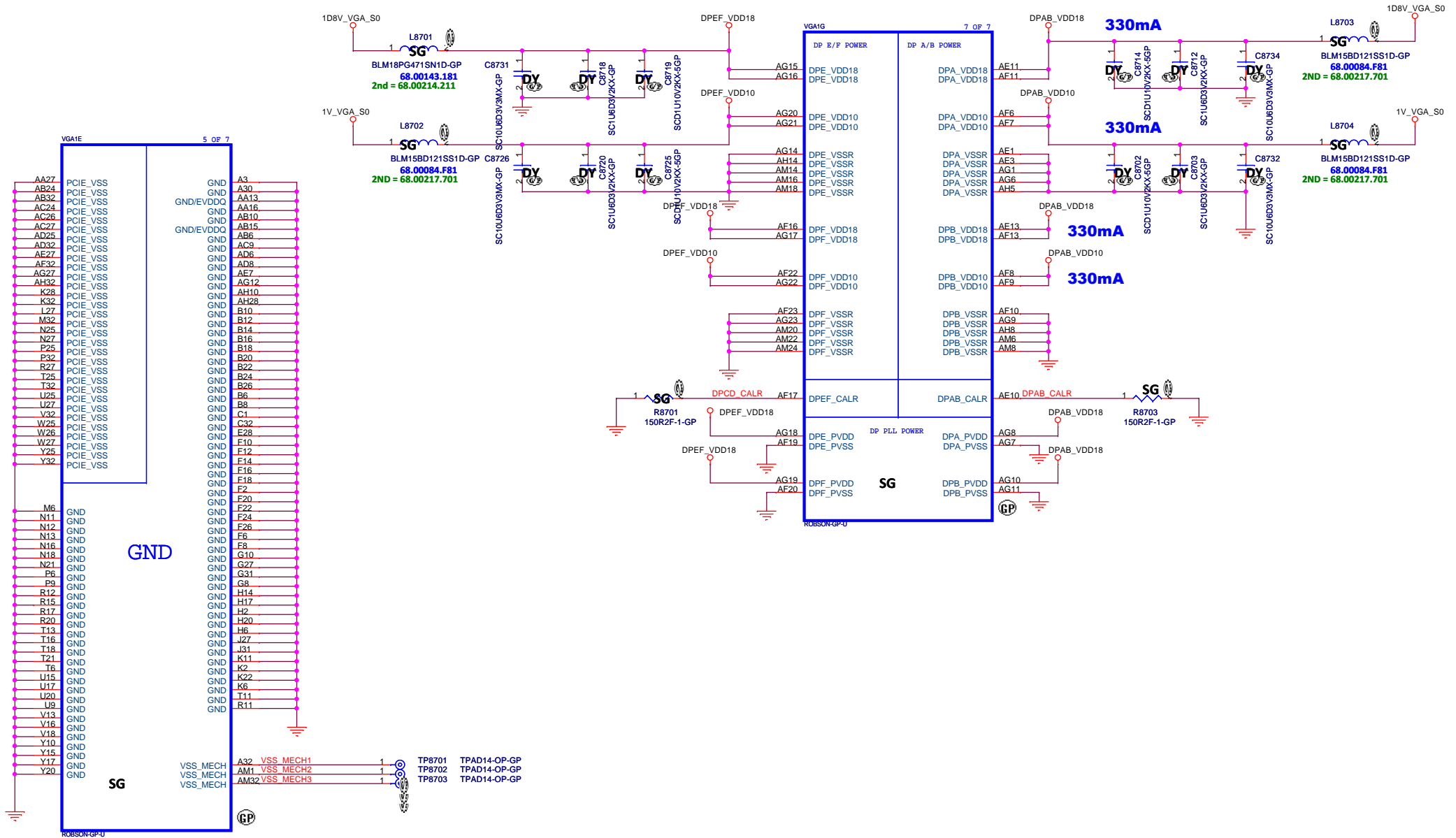
| PX4.0 |       |          |            |           |
|-------|-------|----------|------------|-----------|
| Mode  | PX_EN | PX_EN_1V | PX_EN_VDDC | BIF_VDDC  |
| DIS   | Low   | Low      | High       | VGA_CORE  |
| BACO  | High  | High     | Low        | 1V_VGA_S0 |

|     |  |
|-----|--|
| POP | Q8601, Q8602, R8601, U8601, U8602, U8603<br>U8604, R8603, R8604, R8408 |
| DY  | R8612  |

|     |   |
|-----|---|
| POP | R8612   |
| DY  | Q8601, Q8602, R8601, U8601, U8602, U8603<br>U8604, R8603, R8604, R8605, R8408 |

**SSID = VIDEO**

For Video output port power rail.

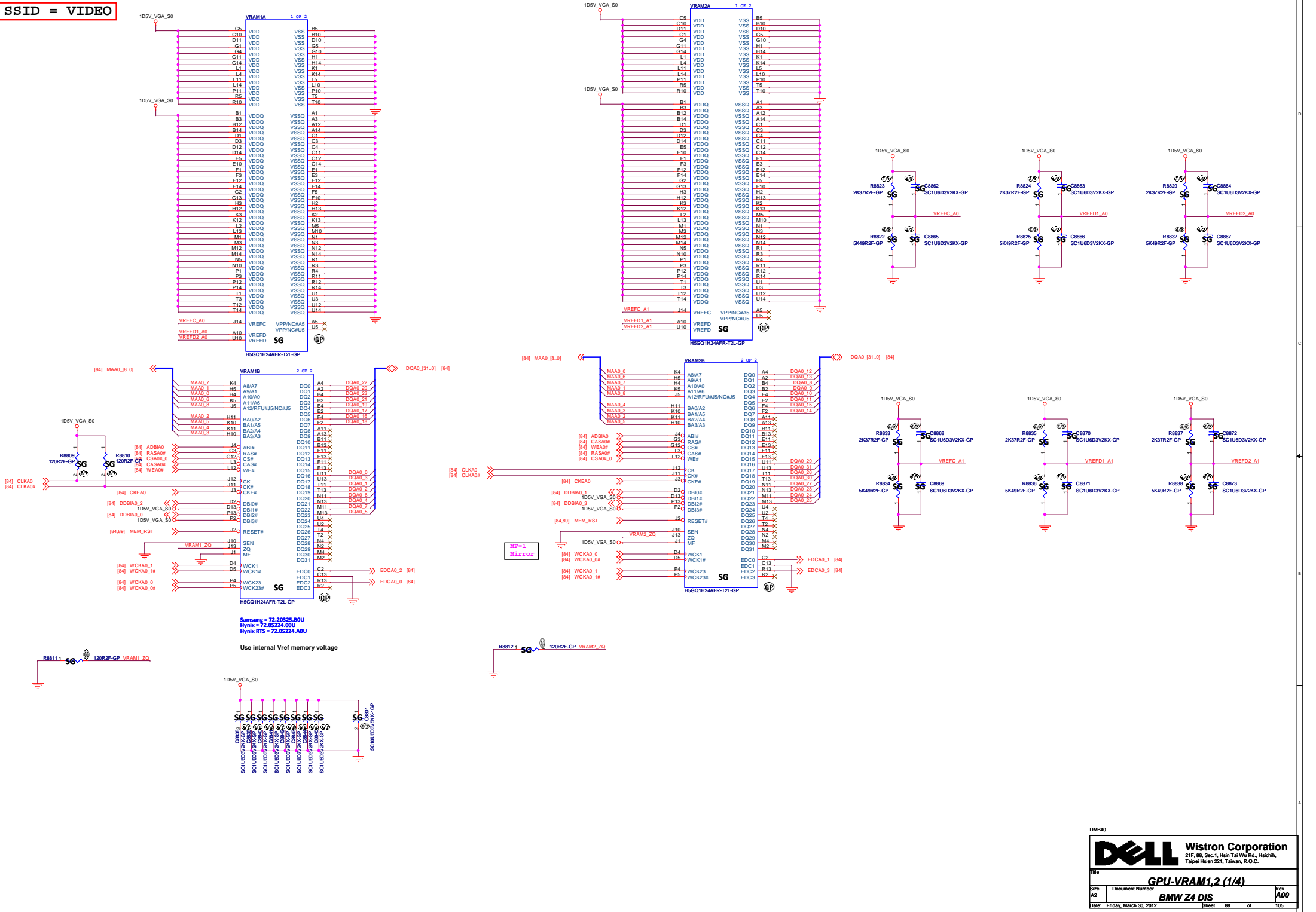


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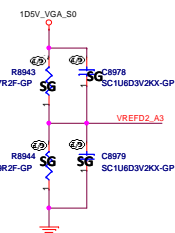
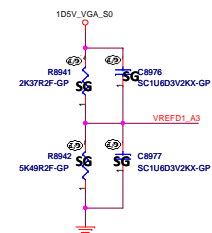
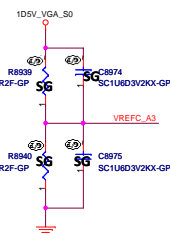
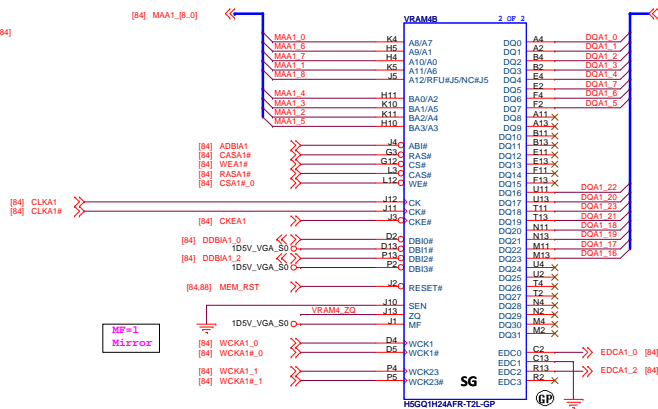
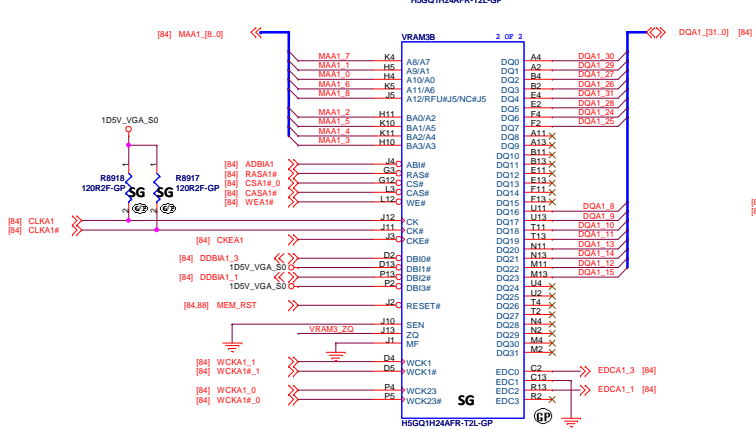
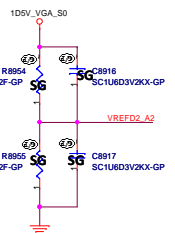
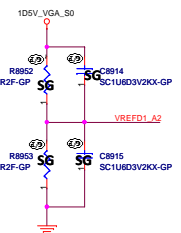
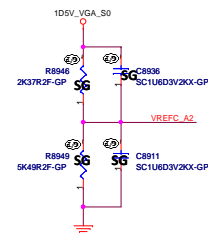
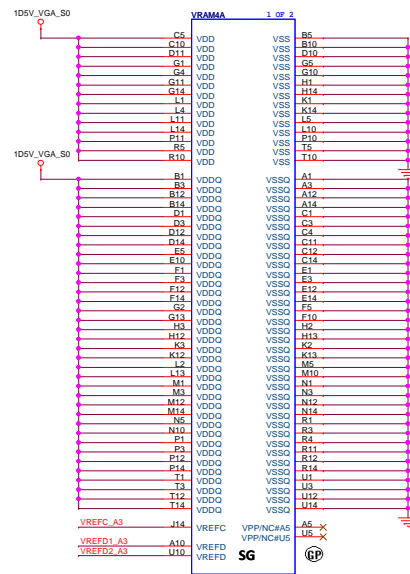
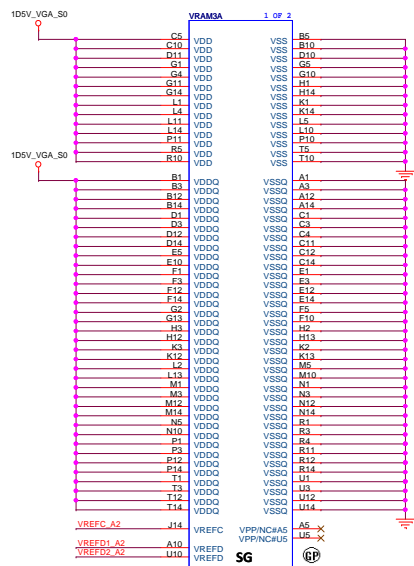
|                           |                        |             |            |
|---------------------------|------------------------|-------------|------------|
| Title                     |                        |             |            |
| <b>GPU DPPWR/GND(5/5)</b> |                        |             |            |
| Size<br>A3                | Document Number        |             | Rev        |
|                           | <b>BMW Z4 DIS</b>      |             | <b>A00</b> |
| Date:                     | Friday, March 30, 2012 | Sheet 87 of | 105        |

SSID = VIDEO



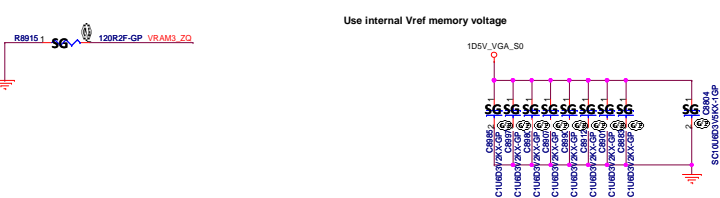


## SSID = VIDEO



Samsung = 72.20325.00U  
Hynix = 72.05224.00U

**Use internal Vref memory voltage**



(Blanking)

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|       |                        |            |                 |        |
|-------|------------------------|------------|-----------------|--------|
| Title |                        |            | <b>Reserved</b> |        |
| Size  | Document Number        | Rev        |                 |        |
| A3    | <b>BMW Z4 DIS</b>      | <b>A00</b> |                 |        |
| Date: | Friday, March 30, 2012 | Sheet      | 90              | of 105 |

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Title

**Reserved**

Size  
A3

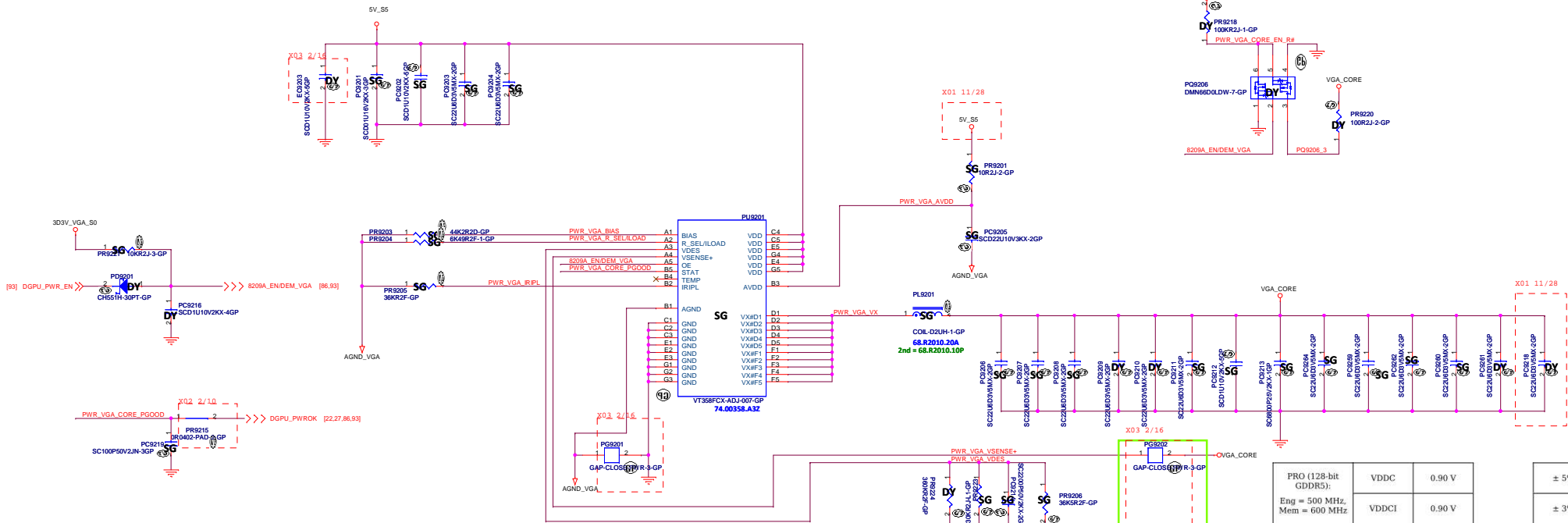
Document Number  
**BMW Z4 DIS**

Rev  
**A00**

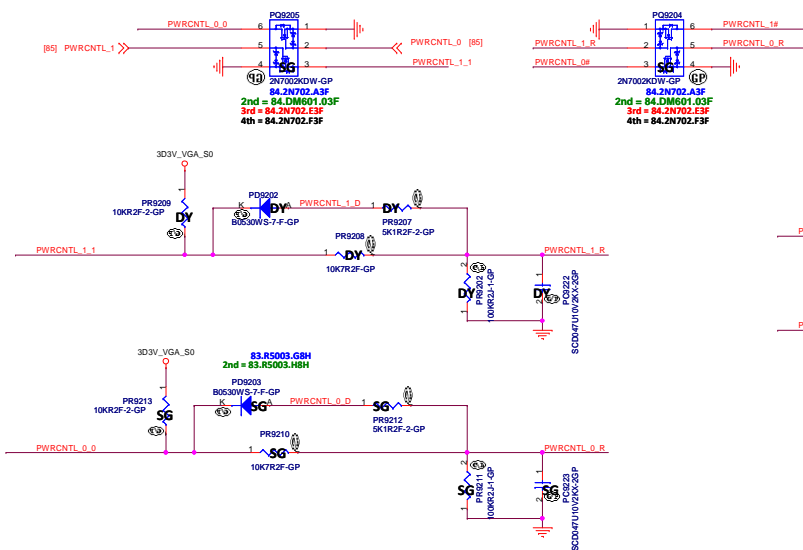
Date: Friday, March 30, 2012

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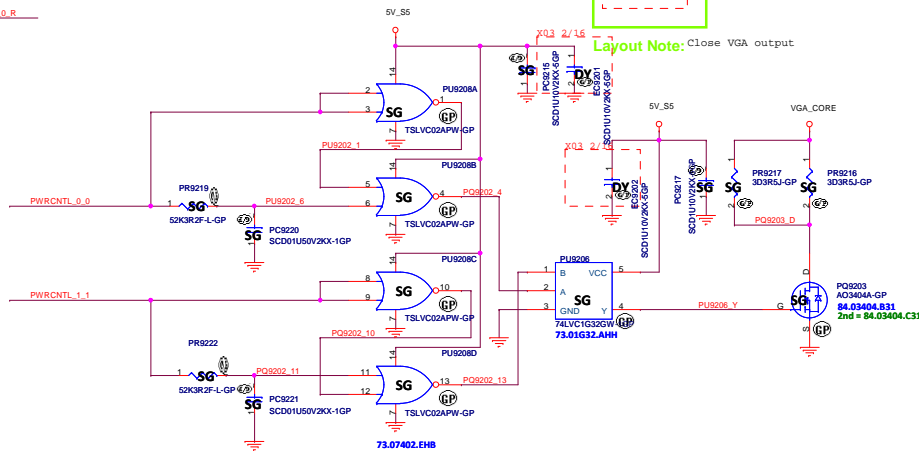
```
SSID = PWR.Plane.Regulator vga core
```



|  |       |        |      |                               |
|--|-------|--------|------|-------------------------------|
| PRO (128-bit<br>GDDR5):<br><br>Eng = 500 MHz,<br>Mem = 600 MHz | VDDC  | 0.90 V | ± 5% | 16.0 A (RMS)<br>22.0 A (Peak) |
|  | VDDCI | 0.90 V | ± 3% | 3.3 A (RMS)<br>3.9 A (Peak)   |



| VID0<br>GPIO15 | Voltage |
|----------------|---------|
| 1              | 1V      |
| 0              | 0.9V    |



◀Core Design▶

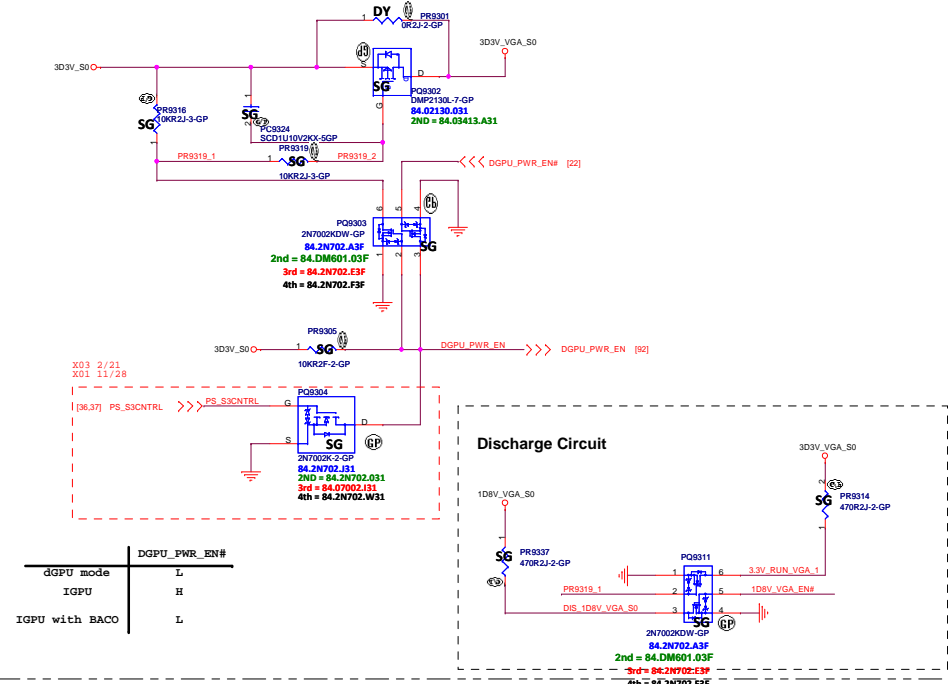


|       |                        |
|-------|------------------------|
| Title | <b>VT357_+VGA_CORE</b> |
|-------|------------------------|

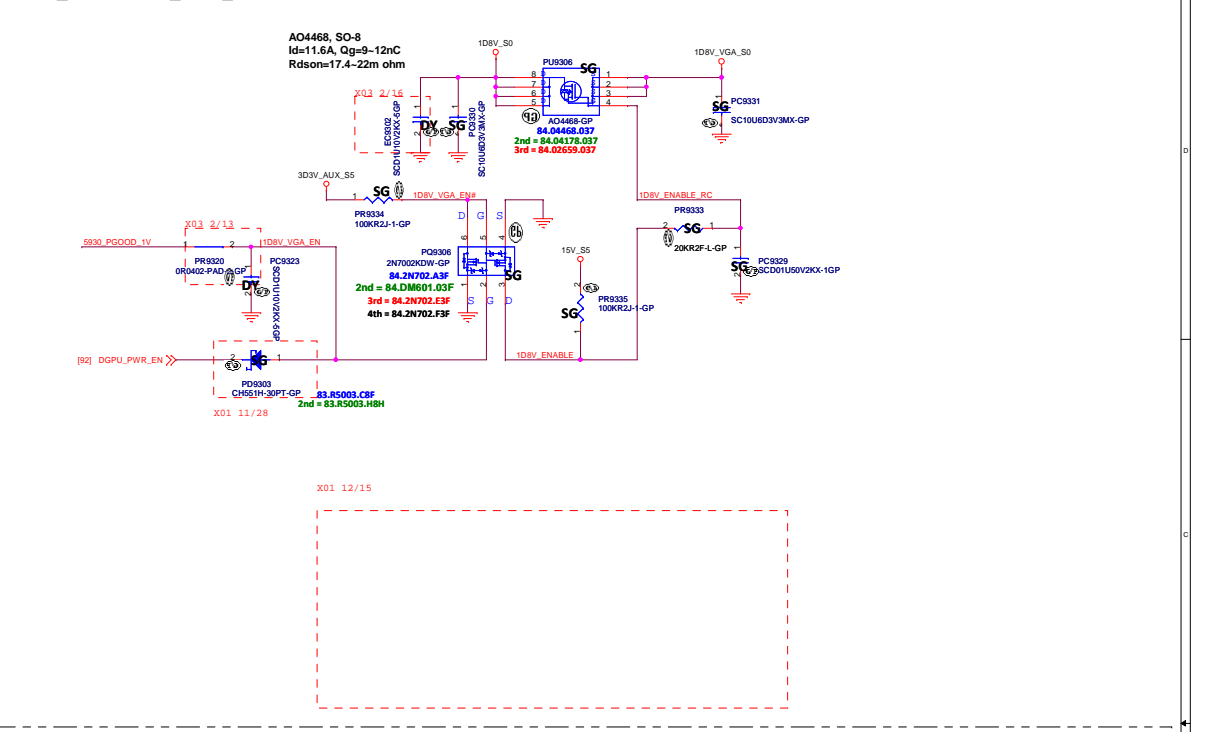
|   |                                      |                   |
|---|--------------------------------------|-------------------|
| Size<br>A2  | Document Number<br><b>BMW Z4 DIS</b> | Rev<br><b>A00</b> |
| Date: Friday, March 30, 2012      Sheet 92 of 105 |                                      |                   |

SSID = PWR.Plane.Regulator\_3p3v\_vga, 1p8v\_vga, 1p5v\_vga, 1v\_vga

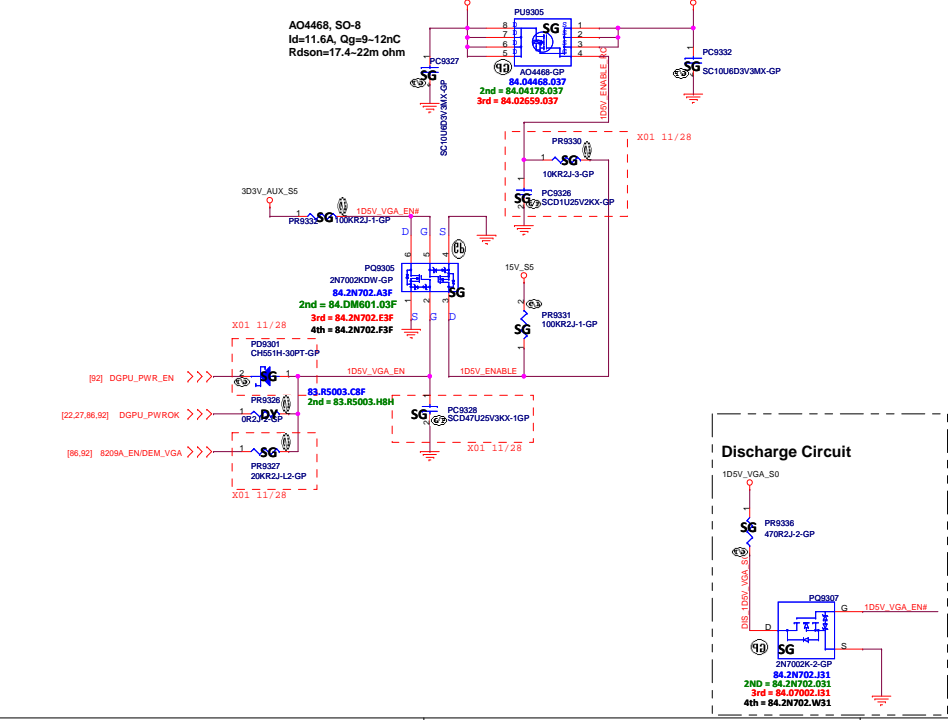
3D3V\_S0 to 3D3V\_VGA\_S0 Transfer



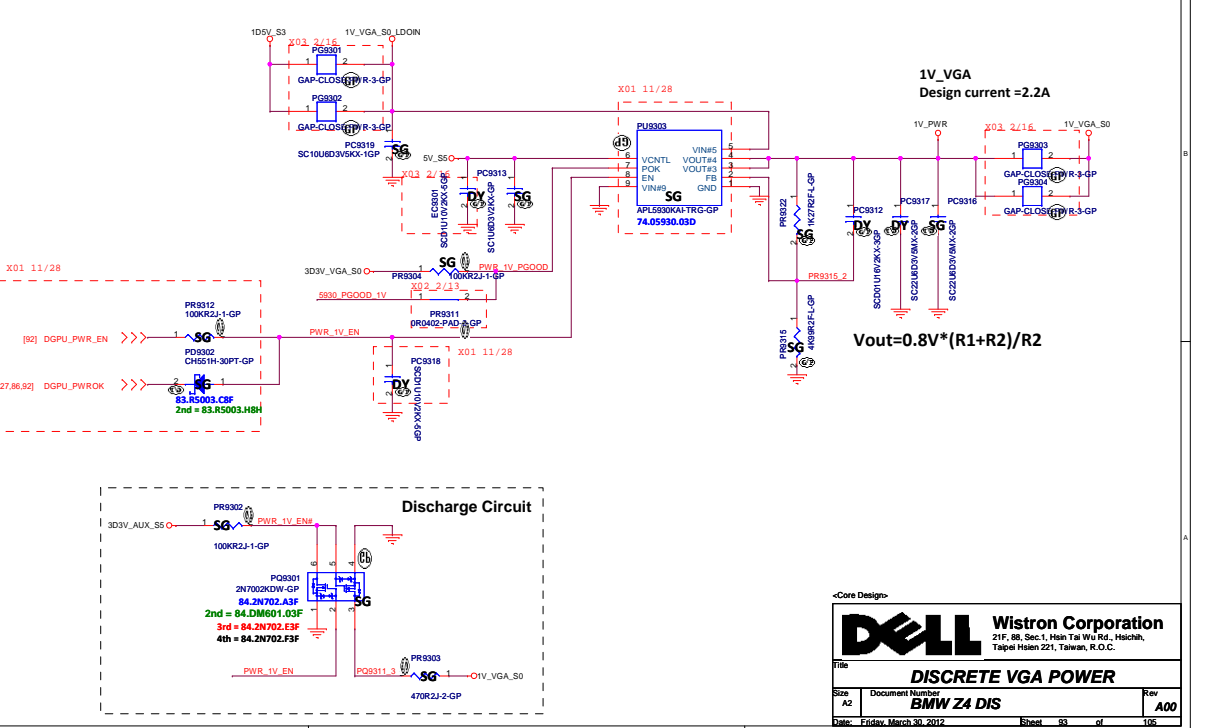
1D8V\_S0 to 1D8V\_VGA\_S0 Transfer



1D5V\_S3 to 1D5V\_VGA\_S0 Transfer



APL5930 for 1V\_VGA\_S0



(Blanking)

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DELL

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Title

Reserved

Size

A3

Document Number

BMW Z4 DIS

Rev


A00

Date: Friday, March 30, 2012

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Title

Reserved

Size  
A3

Document Number  
BMW Z4 DIS


Rev  
A00

Date: Friday, March 30, 2012

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Title

Size  
A3

Document Number  
**BMW Z4 DIS**

Date: Friday, March 30, 2012

**Reserved**

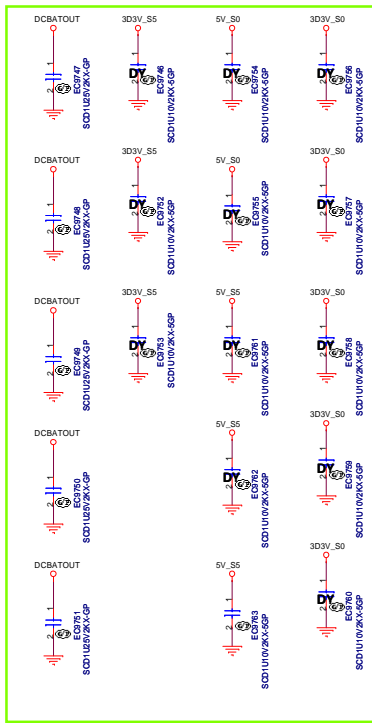
Rev  
**A00**

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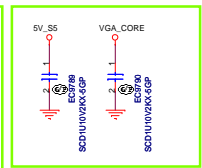


SSID = User.Interface

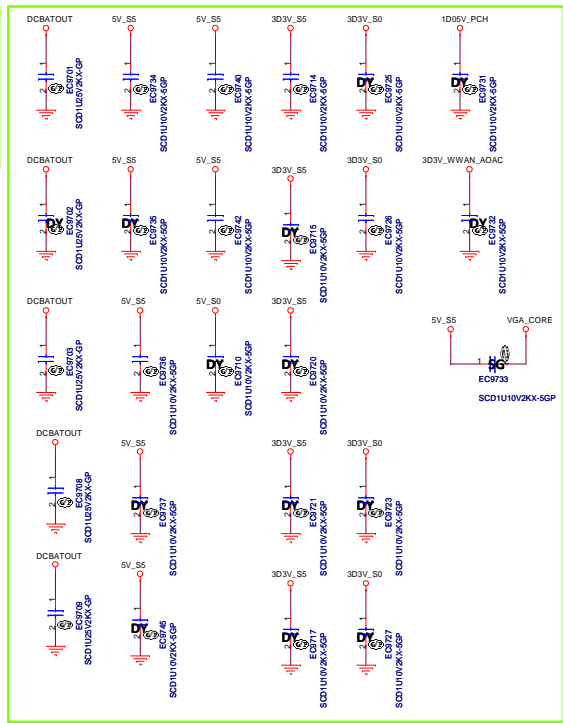
RF



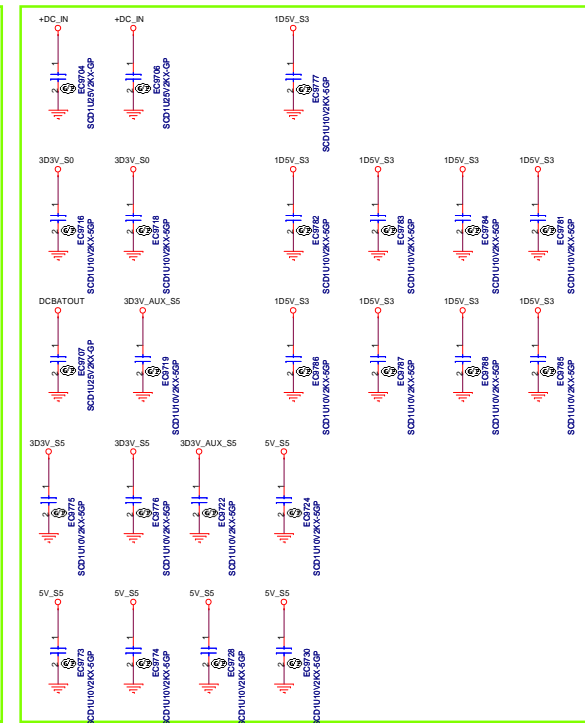
RF X03 2/16



EMI X03 2/13 A00 3/27 A00 3/29

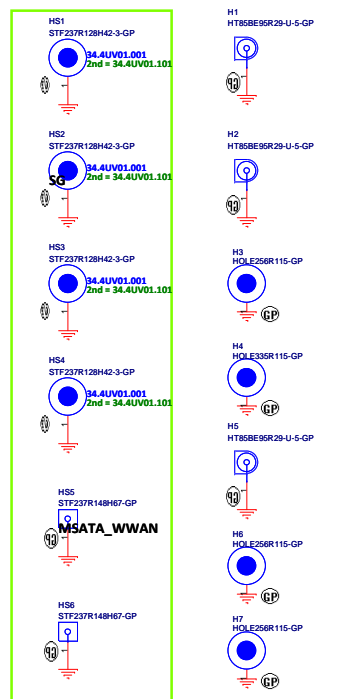


EMI X03 2/16 X03 2/21

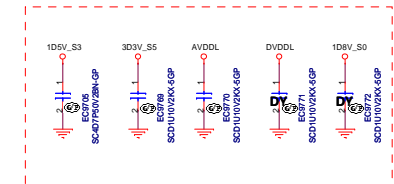


SSID = Mechanical

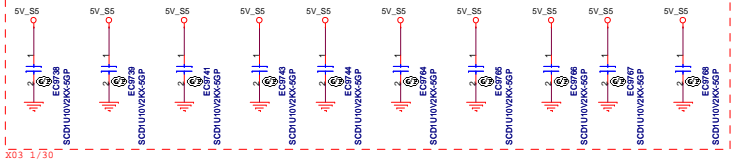
On the TOP side



X01 12/15 For RF



X01 12/09 For EMI X01 12/30



X03 1/30

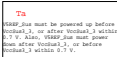


X01 12/23



(AC mode)

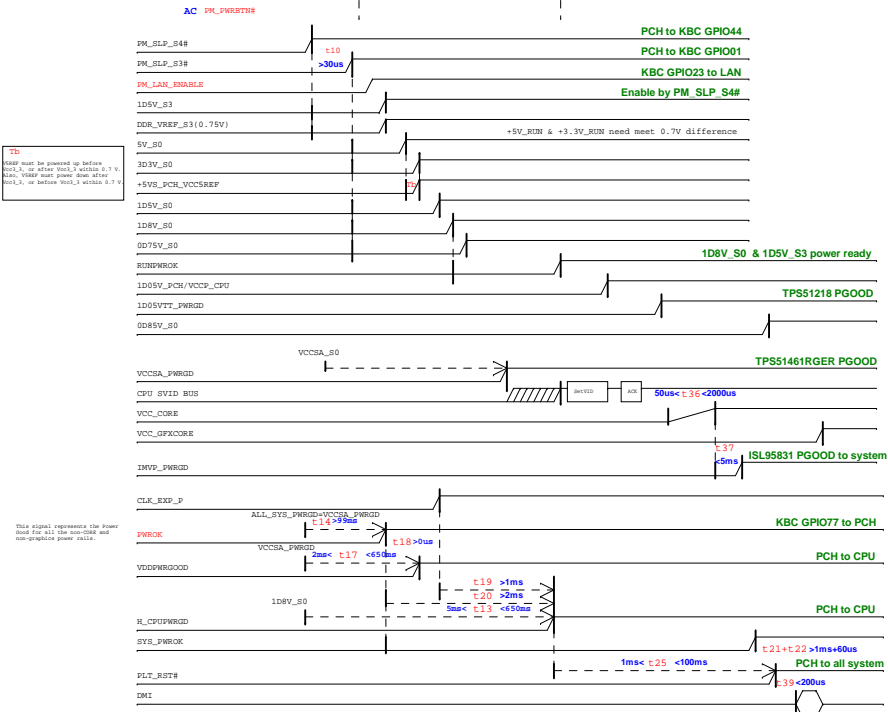
Within logic high level and disable  
it is less than the logic low level.



Not floating.

sense the power button status

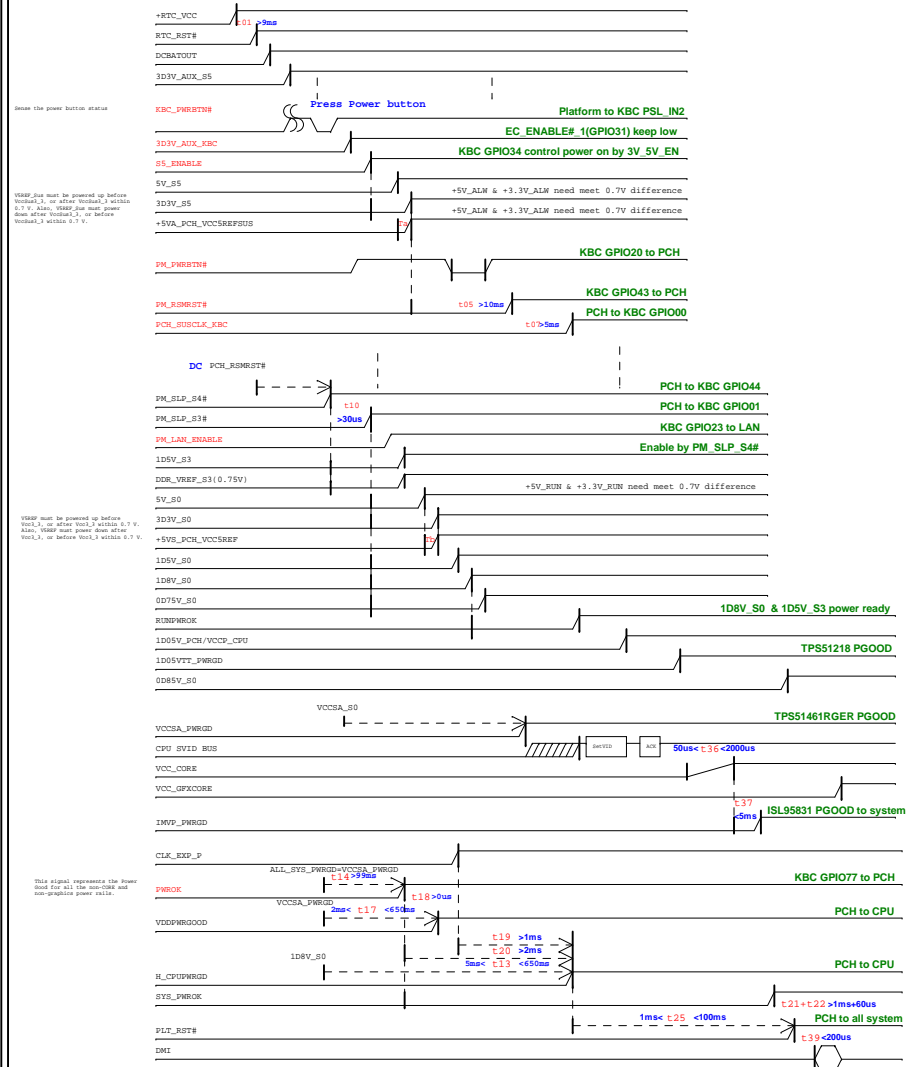
This signal has an internal pull-up resistor and has an internal 16 ns de-bounce on the input.



This signal represents the Power Good for all the non-CORE and non-graphics power rails.

For power-down, reversing the ramp-up sequence is recommended.

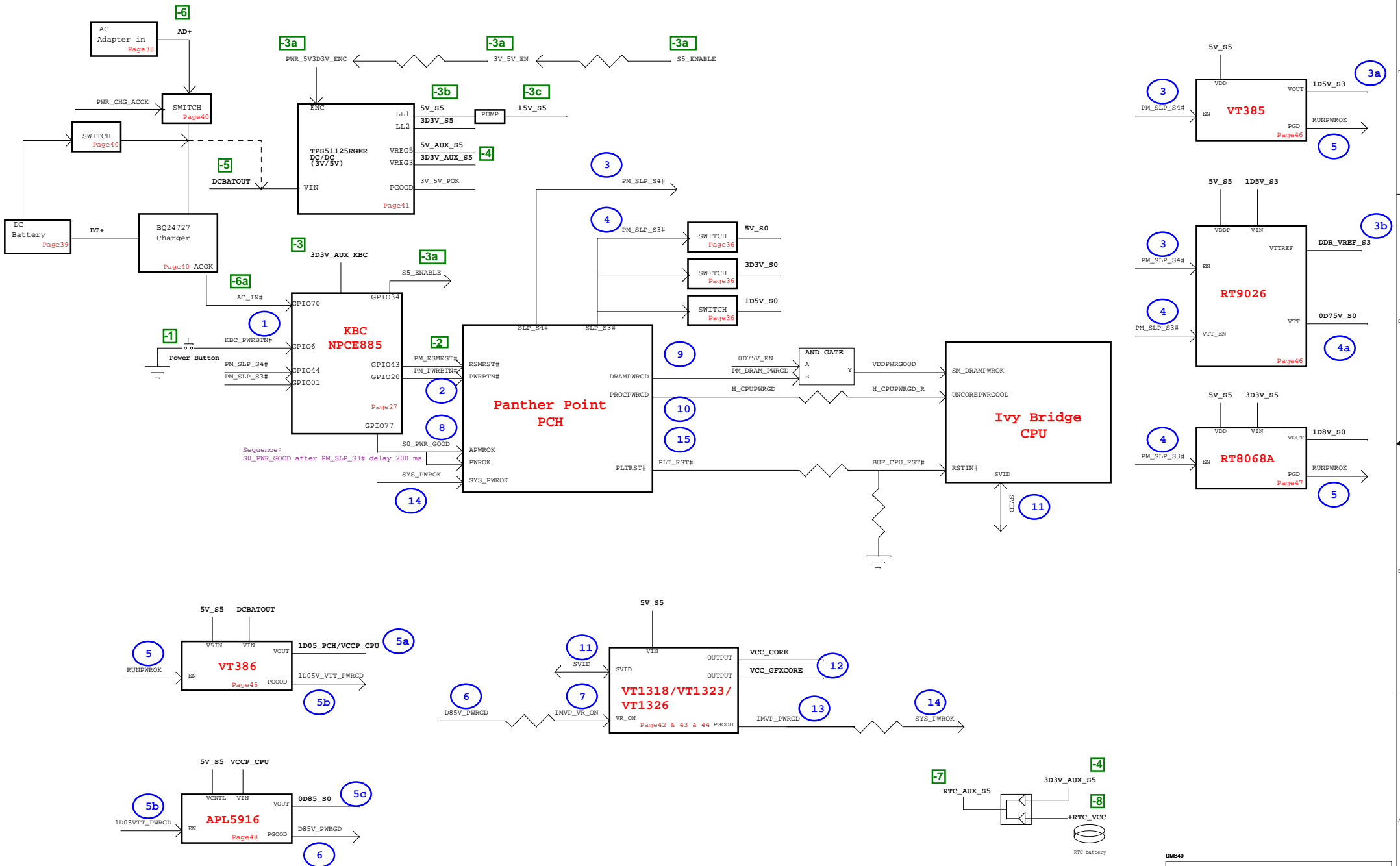
red word: KBC GPIO



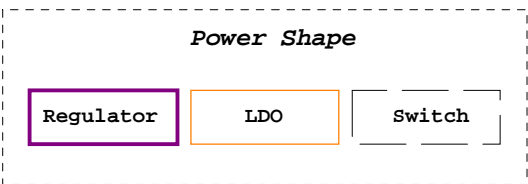
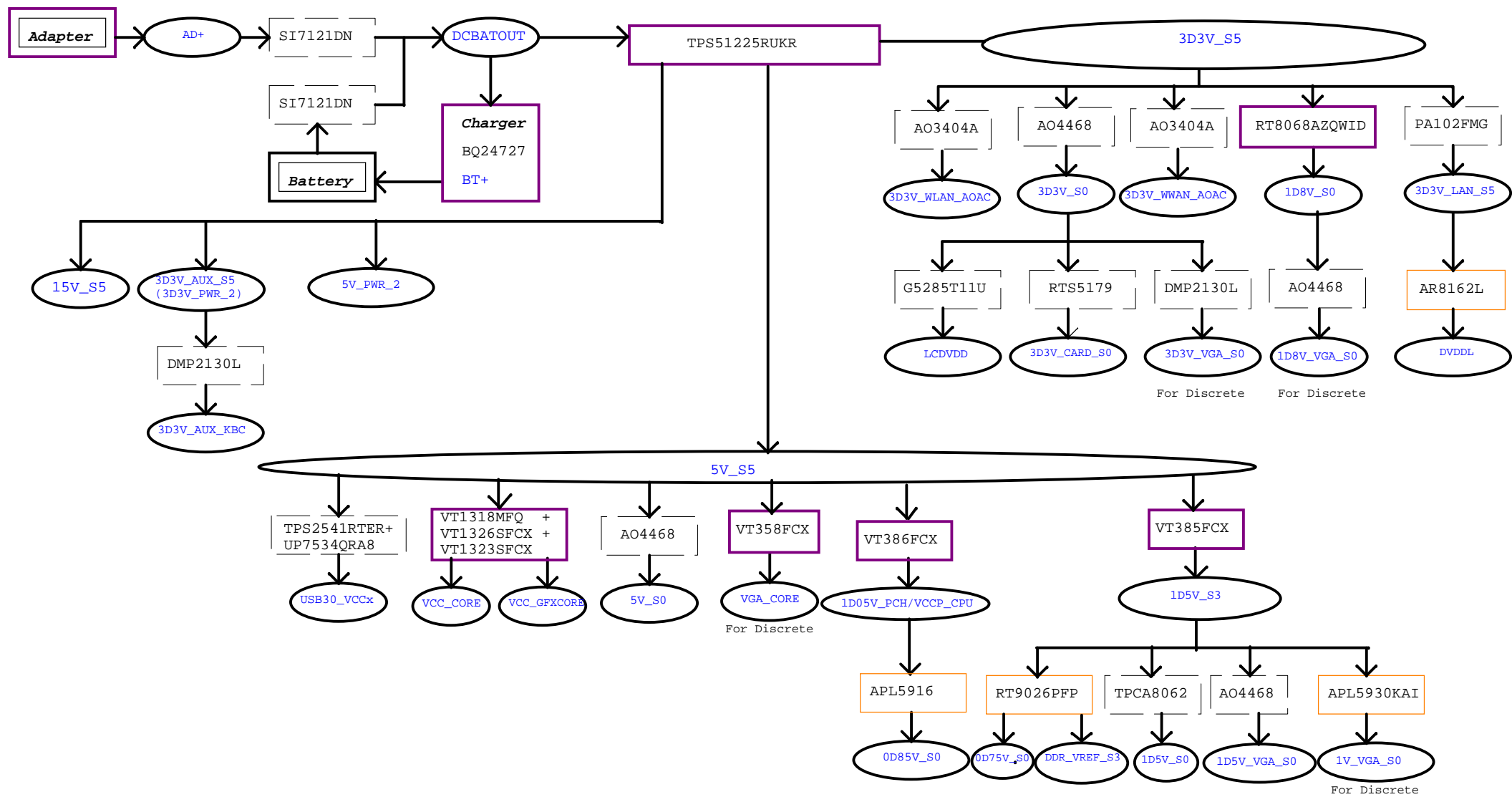
VREF must be powered up before Vcc1\_3, or after Vcc1\_3 within 0.7 V. Also, VREF must power down after Vcc1\_3, or before Vcc1\_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

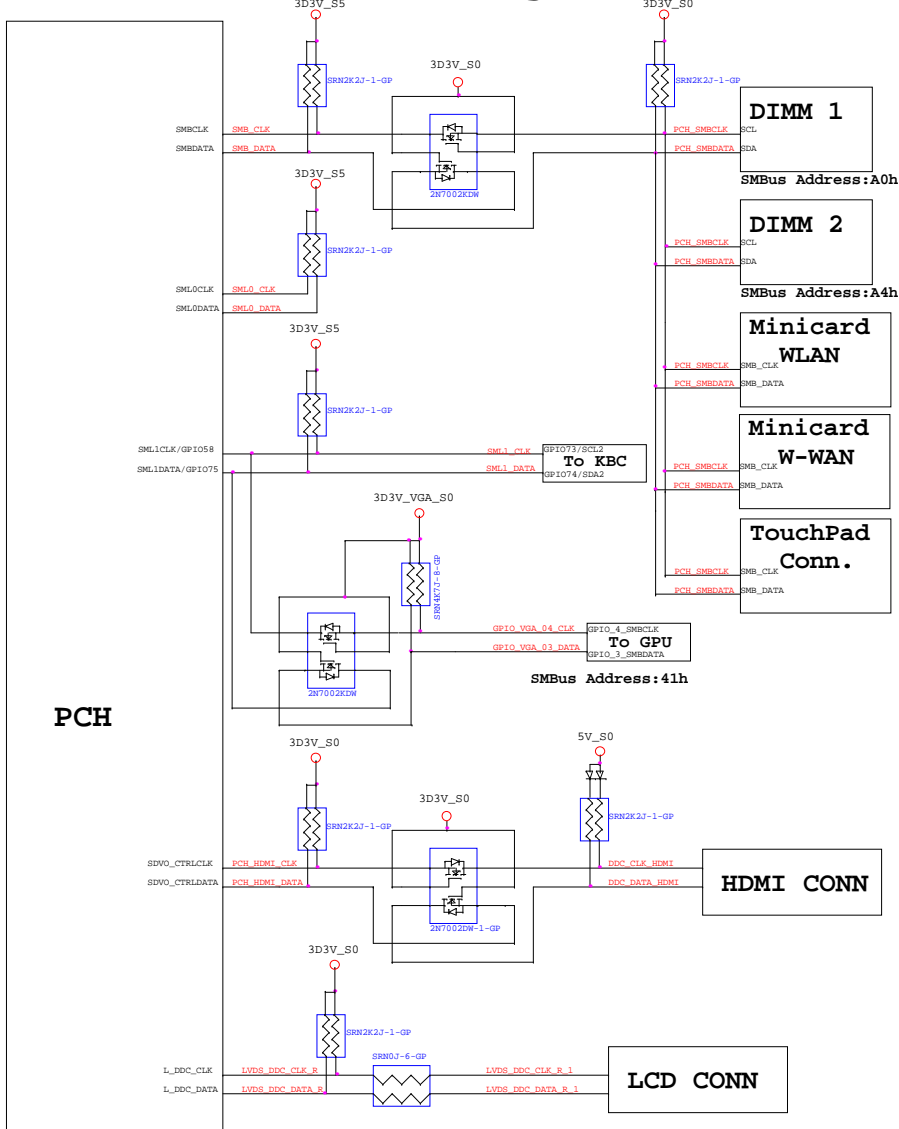
Wistron CHIEF RIVER POWER UP SEQUENCE DIAGRAM



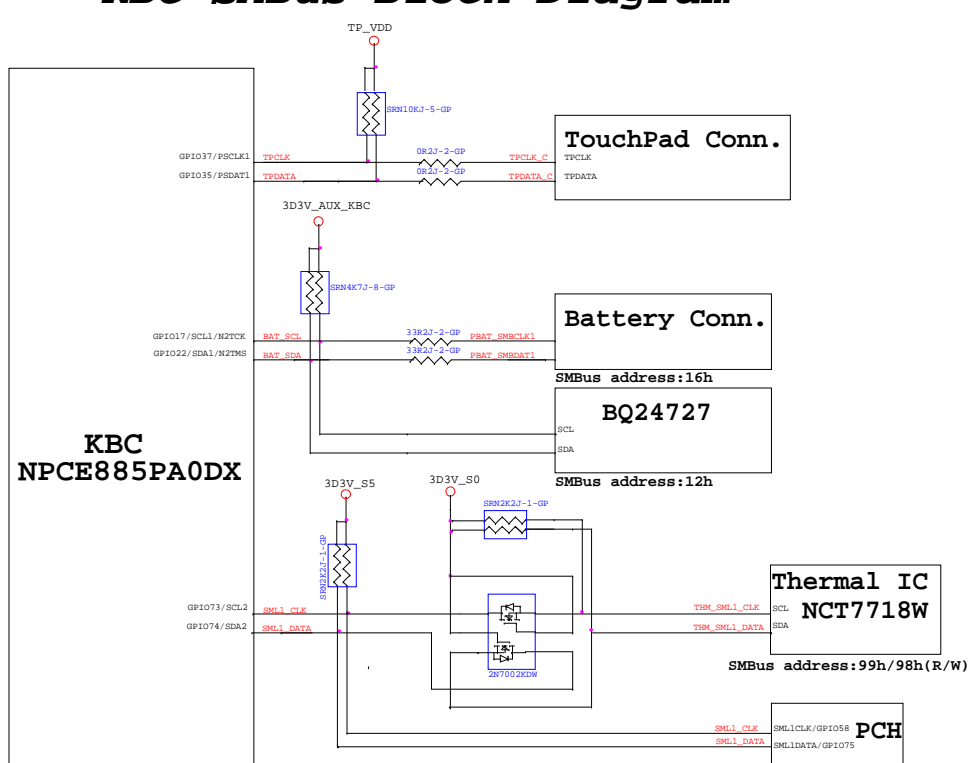
Power Up Sequence: -8 ~ 15



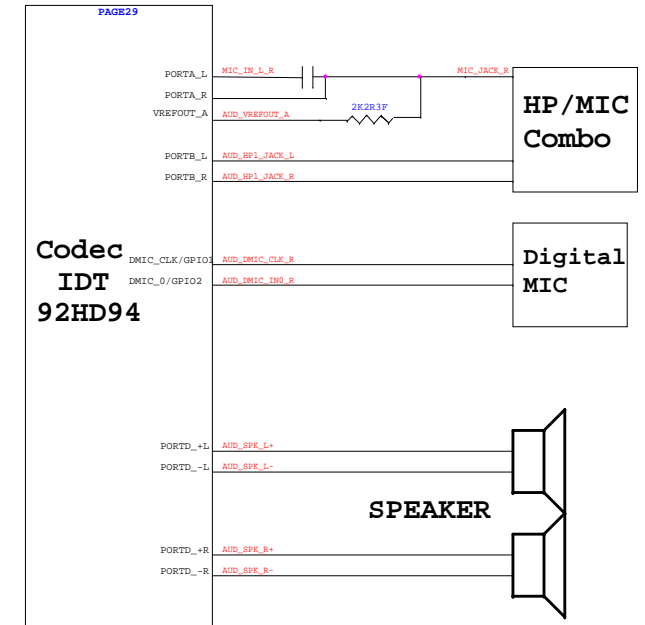
PCH SMBus Block Diagram



KBC SMBus Block Diagram




### Audio Block Diagram



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|------------|------|---|-------|---------|
| 2011 11/28 | 92   | Change VT358 AVDD power rail to 5V_S5 to avoid leakage  | Power | X01     |
| 2011 11/28 | 92   | Re-name Cap PC4663 to PC9218.   | EE    | X01     |
| 2011 11/28 | 85   | Change U8506 power rail and select pin to 3D3V_VGA_S0 to avoid leakage  | EE    | X01     |
| 2011 11/28 | 93   | Change PU9303 to 74.05930.03D by design   | EE    | X01     |
| 2011 11/28 | 93   | POP PD9301, PD9302, PD9303, PD9304, PC9328, change PR9327 to 20K, PR9330 to 10K, PC9326 to 0.1u, PR9312 to 100K, PR9312 re-connect to DGPU_PWR_EN, PD9302 re-connect to DGPU_PWROK for GPU power sequence | EE    | X01     |
| 2011 11/28 | 37   | Change R3714 to 10K to fix step-like waveform   | EE    | X01     |
| 2011 11/28 | 84   | DY R8408 cause GPU support PX5.0  | EE    | X01     |
| 2011 11/28 | 86   | DY R8605, Q8602, R8603, R8604, U8601, U8602, U8603, U8604, cause GPU support PX5.0  | EE    | X01     |
| 2011 12/02 | 27   | Reserved DGPU_PWROK signal to inform KBC  | EE    | X01     |
| 2011 12/02 | 62   | POP R6208, DY R6201 for USB charging function.  | EE    | X01     |
| 2011 12/02 | 85   | Change VRAM type setting.   | EE    | X01     |
| 2011 12/02 | 41   | Change PT4101, PT4103, PT4104 to 77.52271.09L for design change   | EE    | X01     |
| 2011 12/02 | 27   | Add R2737 for avoiding KBC power drop.  | EE    | X01     |
| 2011 12/02 | 37   | Change R3719 to Q402 type   | EE    | X01     |
| 2011 12/02 | 69   | Change TPAD1 conn by ME   | ME    | X01     |
| 2011 12/02 | 82   | Change LEDBD1 conn by ME  | ME    | X01     |
| 2011 12/02 | 56   | Change HDD1 conn by ME  | ME    | X01     |
| 2011 12/02 | 68   | Change PWSW1 conn by ME   | ME    | X01     |
| 2011 12/02 | 27   | Change RSTSW1 conn by ME  | ME    | X01     |
| 2011 12/02 | 39   | Add BATSW1 and R3901 for avoiding MB crack on assembling.   | ME    | X01     |
| 2011 12/02 | 60   | Change RTC1 conn by ME  | ME    | X01     |
| 2011 12/02 | 39   | DY D3901, D3902, D3903 cause the battery is internal type.  | EE    | X01     |
| 2011 12/02 | 51   | Re-name D5001 and F5001 to D5101 and F5101, and DY F5101 and add R5109 due to no current leakage problem  | EE    | X01     |
| 2011 12/02 | 14   | Change DM1 conn by ME   | ME    | X01     |
| 2011 12/02 | 27   | Change R2724 to 20K for X01 version   | EE    | X01     |
| 2011 12/02 | 85   | DY C8523, cause VGA temp detect by SMBUS.   | EE    | X01     |
| 2011 12/02 | 28   | DY U2803, C2817, C2818 cause VGA temp detect by SMBUS.  | EE    | X01     |
| 2011 12/02 | 38   | Del PR3812.   | EE    | X01     |
| 2011 12/02 | 49   | Change LCD1 conn by ME  | ME    | X01     |
| 2011 12/02 | 60   | POP U6001 and del ROMSK1 for X01 version  | EE    | X01     |
| 2011 12/02 | 65   | Change R6507 to J type  | EE    | X01     |
| 2011 12/02 | 39   | Change BATT1 conn by ME   | ME    | X01     |
| 2011 12/02 | 82   | Change IOBD1 conn by ME   | ME    | X01     |
| 2011 12/02 | 68   | Add WLAN/WWAN LED power control circuit   | EE    | X01     |

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|------------|------|--|-------|---------|
| 2011 12/09 | 27   | Change AOAC_PCIE_WAKE# pull high to 3D3V_WLAN_AOAC and PCIE_WAKE# to 3D3V_LAN_S5 | EE    | X01     |
| 2011 12/09 | 66   | Change WWAN power to 3D3V_S0   | EE    | X01     |
| 2011 12/09 | 8    | Change VCC_CORE MLCC by power team request                                       | Power | X01     |
| 2011 12/09 | 9    | Change AXG_CORE MLCC by power team request                                       | Power | X01     |
| 2011 12/09 | 22   | Reserved DGPU_HOLD_RST# & DGPU_PWR_EN# pull high and down                        | EE    | X01     |
| 2011 12/09 | 97   | Follow EMI request added Cap.  | EMI   | X01     |
| 2011 12/09 | 20   | Rename PCIE request pin  | EE    | X01     |
| 2011 12/09 | 65   | Add WLAN requirist circuit   | EE    | X01     |
| 2011 12/12 | 40   | design change PU4001 by Power team request                                       | Power | X01     |
| 2011 12/12 | 41   | design change PU4106 by Power team request                                       | Power | X01     |
| 2011 12/12 | 41   | Change PU4102 to colay symbol by Power team request                              | Power | X01     |
| 2011 12/12 | 45   | Change PU4501to VT386 by Power team request                                      | Power | X01     |
| 2011 12/12 | 46   | Change PR4609 and PR4612 by Power team request                                   | Power | X01     |
| 2011 12/12 | 48   | Change PU4801 by Power team request  | Power | X01     |
| 2011 12/12 | 43   | Reserved PT4301 by Power team request  | Power | X01     |
| 2011 12/12 | 84   | Change R8412 to 4.7k.  | EE    | X01     |
| 2011 12/12 | 27   | Change U2701 to new P/N  | EE    | X01     |
| 2011 12/13 | 82   | Add ER8201, ER8202, ER8203, ER8204 by EMI request.                               | EMI   | X01     |
| 2011 12/13 | 18   | Reserved USB_PN13, USB_PP13 test point.  | EE    | X01     |
| 2011 12/13 | 62   | Del USB3.0 Redriver circuit.   | EE    | X01     |
| 2011 12/13 | 27   | Change R2735 and R2737 to 20K for fix AUX power overshoot.                       | EE    | X01     |
| 2011 12/13 | 41   | Change PC4127 to 4.7uF for fix AUX power overshoot.                              | EE    | X01     |
| 2011 12/13 | 82   | Add ER8205, EC8206 by EMI request.   | EMI   | X01     |
| 2011 12/13 | 46   | Add EL4601, EL4602 by EMI request.   | EMI   | X01     |
| 2011 12/13 | 43   | Add EG4301,EG4302EG4303,EG4304,EG4305,EG4306,EG4307 by EMI request.              | EMI   | X01     |
| 2011 12/13 | 44   | Add EG4401,EG4402,EG4403,EG4404,EG4405,EG4406,EG4407 by EMI request.             | EMI   | X01     |
| 2011 12/13 | 15   | Change DM2 conn by ME request  | ME    | X01     |
| 2011 12/15 | 97   | Add EC9736, EC9726, EC9750 EC9708, EC9709, EC9770, EC9705, EC9769 by RF request. | RF    | X01     |
| 2011 12/15 | 56   | Add EC5601 by RF request.  | RF    | X01     |
| 2011 12/15 | 46   | Add EC4638 by RF request.  | RF    | X01     |
| 2011 12/15 | 31   | Add EC3122 by RF request.  | RF    | X01     |

<Core Design>



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|------------|------|---|-------|---------|
| 2011 12/15 | 14   | Change DM1 P/N to 62.10017.S81  | EE    | X01     |
| 2011 12/15 | 15   | Change DM2 P/N to 62.10017.T01  | EE    | X01     |
| 2011 12/15 | 62   | Del R6201 change by USB detect function                                     | EE    | X01     |
| 2011 12/15 | 65   | DY R6507, U6501 for design change   | EE    | X01     |
| 2011 12/15 | 68   | Add R6809, DY C6802, R6803, D6802, WLAN LED power control by AOAC_WLAN_EN#. | EE    | X01     |
| 2011 12/15 | 8    | Change C825, C830, C831, C832 to 0805 type.                                 | EE    | X01     |
| 2011 12/15 | 9    | Change C906, C907, C908, C909, C910 to 0805 type.                           | EE    | X01     |
| 2011 12/15 | 93   | Del 1D8V_VGA_S0 power good circuit.   | EE    | X01     |
| 2011 12/15 | 83   | Del VGA_RST# circuit.   | EE    | X01     |
| 2011 12/15 | 86   | Del 1D5V_VGA_S0 power good circuit.   | EE    | X01     |
| 2011 12/15 | 31   | Reserved EC3101 by RF request.  | RF    | X01     |
| 2011 12/15 | 97   | Reserved EC9771, EC9772 by RF request.                                      | RF    | X01     |
| 2011 12/16 | 86   | Change C8642, C8650, C8647 to 22u 0805 size.                                | EE    | X01     |
| 2011 12/16 | 62   | Pop TR6204, DY R6279, R6280.  | EMI   | X01     |
| 2011 12/16 | 49   | Pop TR4902, DY R4903, R4906.  | EMI   | X01     |
| 2011 12/16 | 8    | Change C847 to 22u 0805 size.   | EE    | X01     |
| 2011 12/16 | 68   | Pop C6802, for soft start.  | EE    | X01     |
| 2011 12/19 | 38   | Change PC3806 to 0805 type  | Power | X01     |
| 2011 12/19 | 43   | Del PT4301 cause no layout area.  | Power | X01     |
| 2011 12/20 | 44   | Change PWR_GFX to PWR_CPU   | Power | X01     |
| 2011 12/20 | 18   | Change touch panel USB signal to port 4.                                    | EE    | X01     |
| 2011 12/20 | 82   | Reserved TPAN1, and swap IOBD1's main and 2nd source.                       | EE    | X01     |
| 2011 12/20 | 49   | Swap LCD1's main and 2nd source.  | EE    | X01     |
| 2011 12/20 | 14   | Change R1401, R1402 to short pad  | EE    | X01     |
| 2011 12/20 | 15   | Change R1502 to short pad   | EE    | X01     |
| 2011 12/20 | 39   | Change R3902, R3903, R3904 to 100 ohm to avoid break KBC when battery in.   | EE    | X01     |
| 2011 12/20 | 27   | Del RN2703, add R2714, R2715.   | EE    | X01     |
| 2011 12/21 | 48   | POP PR4814, change PR4811 to 365ohm, PR4813 to 100Kohm                      | Power | X01     |
| 2011 12/21 | 21   | Add R2115 and del R6001 for SPI louting setting                             | EE    | X01     |
| 2011 12/21 | 8    | DY C807, C843, C824.  | Power | X01     |
| 2011 12/21 | 42   | Change PR4236 to 374ohm, PR4249 to 7.68Kohm.                                | Power | X01     |
| 2011 12/21 | 43   | Change PU4301 IC to lastly version.   | Power | X01     |
| 2011 12/21 | 44   | Change PU4401 IC to lastly version.   | Power | X01     |
| 2011 12/21 | 40   | Design change PU4002 by power request                                       | Power | X01     |
| 2011 12/21 | 27   | Add R2716 to modify PSL circuit.  | EE    | X01     |
| 2011 12/23 | 82   | Swap USB1, USB10 signal to TR8202 TR8201 for layout                         | EE    | X01     |

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|------------|---|---|-------|---------|
| 2011 12/23 | 62  | Swap USB0 signal to TR6204 for layout   | EE    | X01     |
| 2011 12/23 | 97  | Del H8.   | ME    | X01     |
| 2011 12/27 | 51  | Pop D5101, DY R5109.  | EE    | X01     |
| 2011 12/30 | 93  | Change PD9301, PD9302, PD9303, PD9304's 2nd source to 83.R5003.H8H  | EE    | X01     |
| 2011 12/30 | 31  | Change U3101 to 71.08162.A03 due to vendor update new version.  | EE    | X01     |
| 2011 12/30 | 97  | Pop EC9738, EC9739, EC9741, EC9743, EC9744, EC9764, EC9765, EC9766, EC9767, EC9768  | EMI   | X01     |
| 2011 12/30 | 36, 93  | Change U3601 U3602 PU9305 PU9306 2nd to 84.04178.037  | Power | X01     |
| 2011 12/30 | 49  | Change TR4902 to 69.10103.041   | EMI   | X01     |
| 2012 01/09 | 15, 24  | DY C1507 and C2403 by PI testing result.  | EE    | X01     |
| 2012 01/09 | 48  | Change VCCSA to LDO type.   | Power | X02     |
| 2012 01/09 | 51  | Change HDMI SMBUS pull up power to 5V_HDMI_S0_R   | EE    | X03     |
| 2012 01/30 | 48  | Reserved PC4818 PC4819 to prevent VCCSA power IC VID setting(PWM solution)  | EE    | X03     |
| 2012 01/30 | 68  | Add D6803 to fix DW1703 BT LED behavior. and change WLAN LED power rail to 5V_S0.   | EE    | X03     |
| 2012 01/30 | 97, 38  | Take off EC9704, del PS_ID_R.   | EE    | X03     |
| 2012 01/30 | 82  | Move IO BD conn signal for coaxial cable  | EE    | X03     |
| 2012 01/30 | 66  | DY R6615.   | EE    | X03     |
| 2012 01/30 | 40, 38  | Change PR4004 to 3K and PR3816 to 3.3K for hiccup mode adaptor.   | EE    | X03     |
| 2012 01/30 | 62  | Change U6201 to lastly version.   | EE    | X03     |
| 2012 01/30 | 31  | Change L3101 to prevent the shortage problem.   | EE    | X03     |
| 2012 02/06 | 82  | Change TPAN1 P/N by ME request and modify conn pin define.  | EE    | X03     |
| 2012 02/06 | 31  | Reserved C3110 for Lan IC.  | EE    | X03     |
| 2012 02/06 | 5, 8, 9, 14, 15, 19, 23, 24, 27, 28, 36, 37, 38, 49, 51, 62, 65, 66, 83, 85 | Change R504, R812, R909, R1404, R1405, R1505, R1503, R1921, R1916, R1924, R1929, R1925, R2304, R2301, R2307, R2306, R2308, R2403, R2404, R2412, R2402, R2702, R2765, R2794, R2778, R2792, R2733, R2767, R2768, R2720, R2764, R2723, R2727, R2807, R3614, R3710, PR3819, R4912, R4913, R5125, R5101,R5102, R5149, R5103, R5108, R5107, R5106, R5105, R6202, R6203, R6204, R6205, R6505, R6502, R6616, R8322, R8504, R8506, R8507, to short pad | EE    | X03     |
| 2012 02/10 | 41, 42, 45, 46, 47, 95  | Change PR4127, PR4130, PR4133, PR4116, PR4251, PR4250, PR4212, PR4207, PR4228, PR4523, PR4522, PR4510, PR4511, PR4626, PR4621, PR4622, PR4623, PR4611, PR4602, PR4702 ,PR9215 to short pad  | Power | X03     |
| 2012 02/13 | 51  | Change HDMI output power design   | EE    | X03     |
| 2012 02/13 | 41, 42, 18 19, 28, 93   | Change PR9311, PR9320, PR4116, PR4219, PR4223, PR4252, PR4254, PR4261, R1823, R1927 R2813 to short pad  | Power | X03     |
| 2012 02/13 | 97  | Add EC9704, EC9706, EC9716, EC9718, EC9722, EC9724, EC9728, EC9730, EC9775, EC9776, EC9773, EC9774,EC9701, EC9751, EL4901 by EMI required   | EMI   | X03     |



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